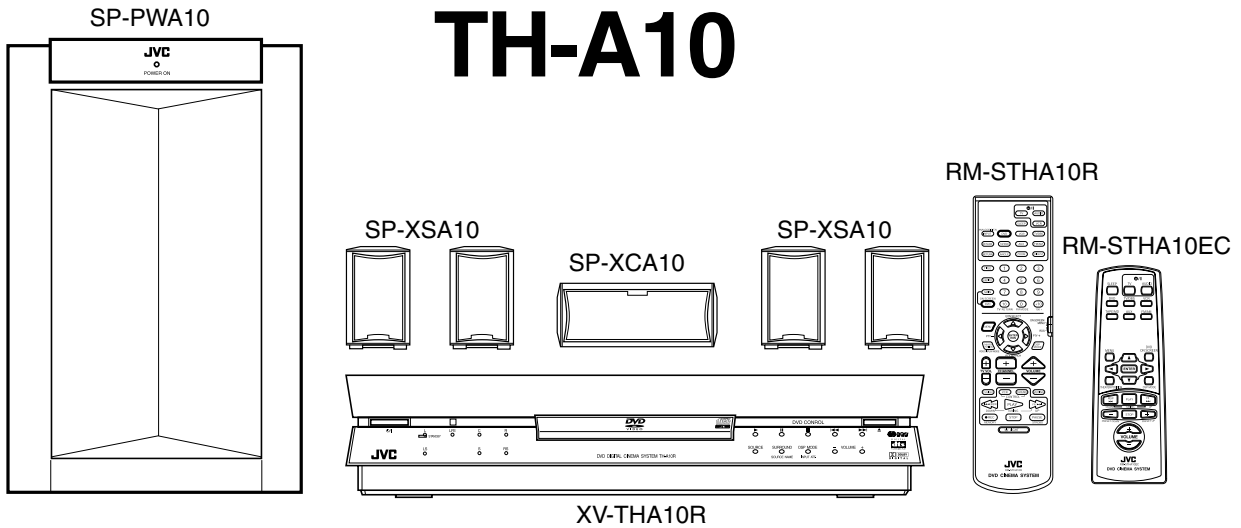


JVC

SERVICE MANUAL

DVD DIGITAL THEATER SYSTEM

TH-A10R TH-A10



**Area Suffix
TH-A10R**
 B U.K.
 EN Northern Europe
 EE Russia

**Area Suffix
TH-A10**
 E Continental Europe

TH-A10R TH-A10	XV-THA10R (DVD player)/XV-TH-A10	
	SP-THA10 (Speaker section)	SP-PWA10 (Powered subwoofer)
		SP-XCA10 (Center speaker)
		SP-XSA10 (Satellite speaker) x 4

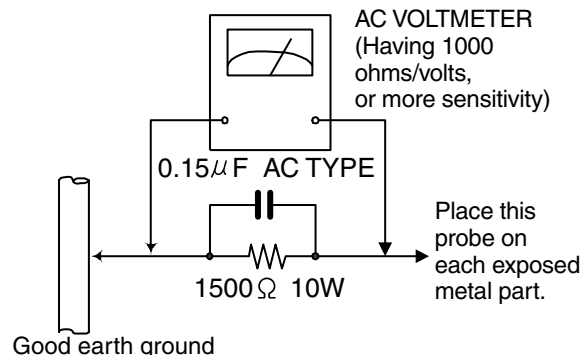
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Safety precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer's warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (Δ) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
5. Leakage current check (Electrical shock hazard testing)
After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock. Do not use a line isolation transformer during this check.

- Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.)
- Alternate check method
Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500 Ω 10W resistor paralleled by a 0.15 μ F AC-type capacitor between an exposed metal part and a known good earth ground. Measure the AC voltage across the resistor with the AC voltmeter.
Move the resistor connection to each exposed metal part, particularly any exposed metal part having a return path to the chassis, and measure the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. voltage measured Any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

CAUTION Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of performing repair of this system.

Preventing static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

1.1. Grounding to prevent damage by static electricity

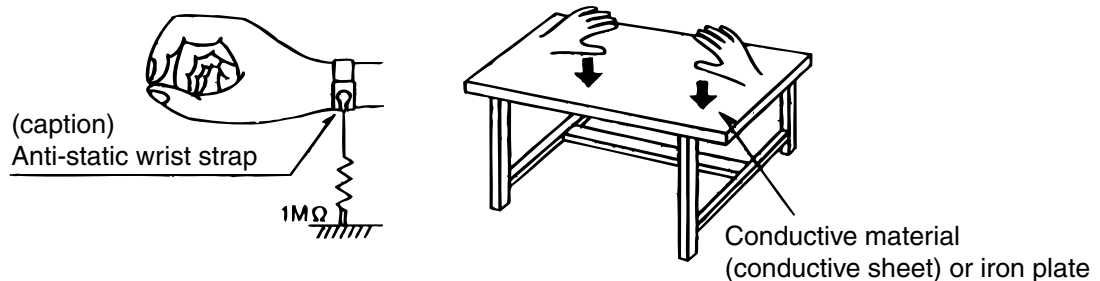
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as DVD players. Be careful to use proper grounding in the area where repairs are being performed.

1.1.1. Ground the workbench

1. Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

1.1.2. Ground yourself

1. Use an anti-static wrist strap to release any static electricity built up in your body.



1.1.3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)
2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

1.2. Handling the traverse unit (optical pickup)

1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.
2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.
3. Handle the flexible cable carefully as it may break when subjected to strong force.
4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

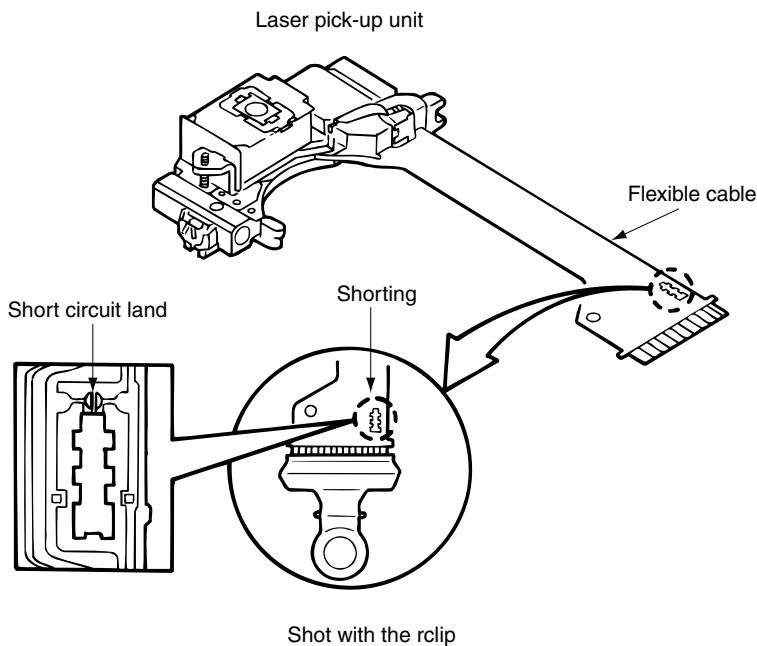
Dismantling and assembling the traverse unit

1. Notice regarding replacement of optical pickup

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs to the optical pickup or connected devices.

(Refer to the section regarding anti-static measures.)

1. Do not touch the area around the laser diode and actuator.
2. Do not check the laser diode using a tester, as the diode may easily be destroyed.
3. It is recommended that you use a grounded soldering iron when shorting or removing the laser diode.
Recommended soldering iron: HAKKO ESD-compatible product
4. Solder the land on the optical pickup's flexible cable.
 - Note : Short the land after shorting the terminal on the flexible cable using a clip, etc., when using an ungrounded soldering iron.
 - Note : After shorting the laser diode according to the procedure above, remove the solder according to the text explanation.



Disassembly method

<Main body>

■ Removing the top cover

(See Fig.1 and 2)

1. Remove the four screws A attaching the top cover (Use an Allen wrench).
2. Lift up the front part of the top cover to release the two joints a and remove the top cover toward the front.

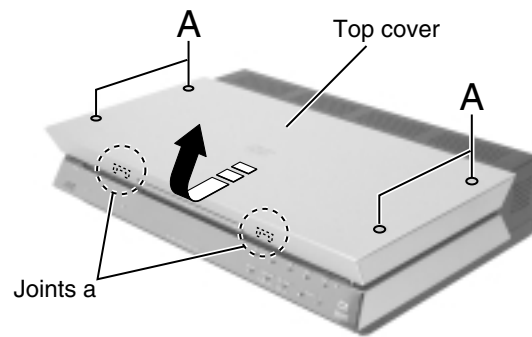


Fig.1

■ Removing the rear cover (See Fig. 3)

- Prior to performing the following procedure, remove the top cover.

1. Remove the four screws B attaching the rear cover on the back of the body. Pull out the rear cover backward.

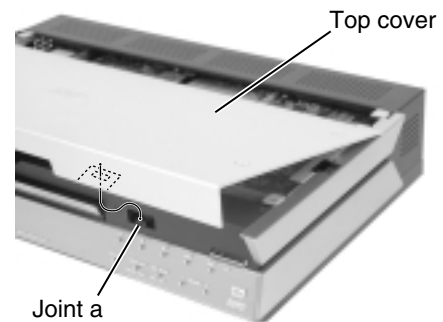


Fig.2

■ Removing the right and left side covers (See Fig. 4 and 5)

- Prior to performing the following procedure, remove the top cover and the rear cover.

1. Move the left side cover backward to release the five joint hooks b and remove the left side cover outward.
2. Remove the right side cover in the same way.

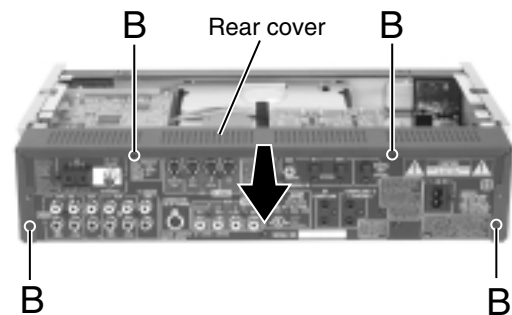


Fig.3

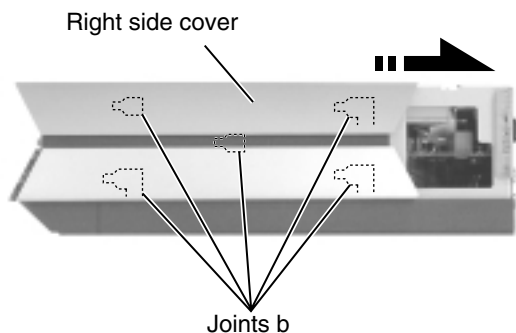


Fig.5

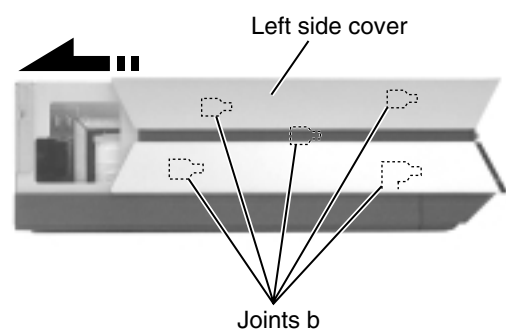


Fig.4

**■Removing the front panel assembly
(See Fig. 6 to 9)**

- Prior to performing the following procedure, remove the top cover, the rear cover and the side covers.
1. Disconnect the harness from connector CN802 on the main board on the upper side of the body.
 2. Remove the two screws C on the upper side of the body.
 3. Remove the three screws D on the bottom of the body.
 4. Release the five joints c and detach the front panel assembly toward the front.

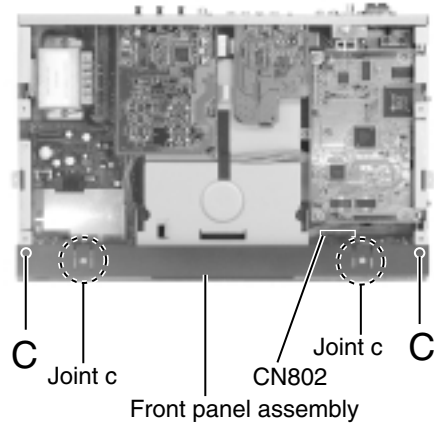


Fig.6

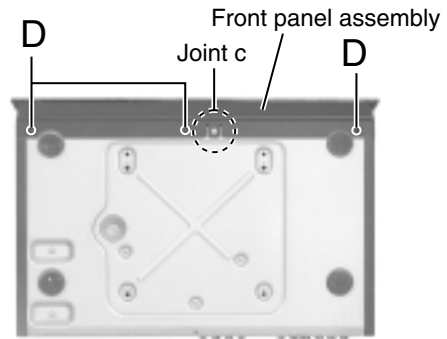


Fig.7

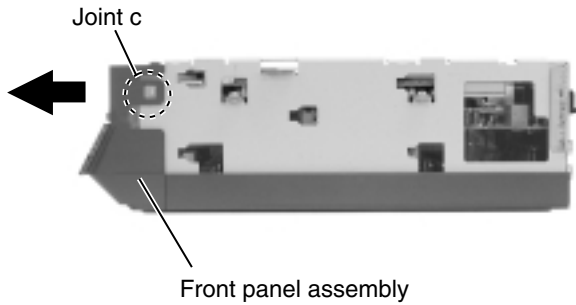


Fig.9

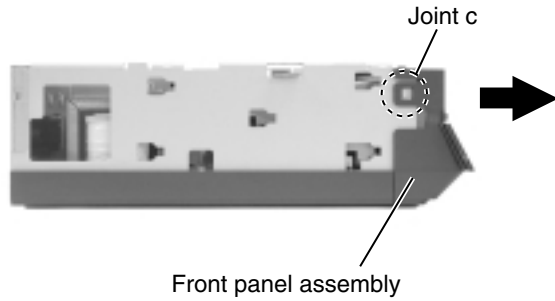


Fig.8

■Removing the right and left corner covers (See Fig.10 and 11)

- Prior to performing the following procedure, remove the top cover, the rear cover, the side covers and the front panel assembly.
- It is not necessary to remove the front panel assembly.

1. Move the left corner cover backward to release the three joint hooks d.
2. Remove the right corner cover in the same way.

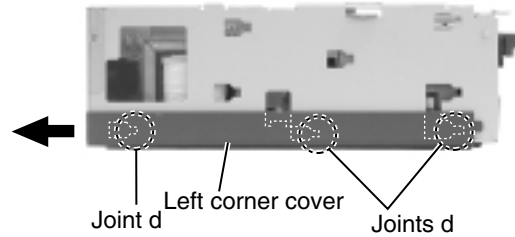


Fig.10

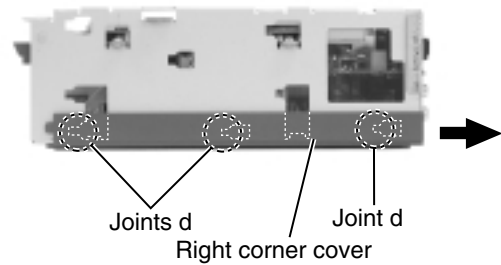


Fig.11

■Removing the rear panel (See Fig.12 to 14)

- Prior to performing the following procedure, remove the top cover and the rear cover.

1. Remove the eighteen screws E and the one screw F attaching the rear panel.
2. Release the two joints e on both sides of the body.

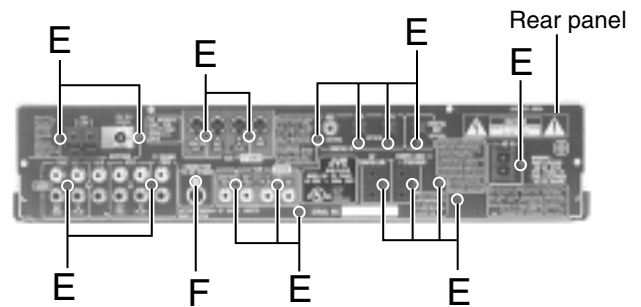


Fig.12

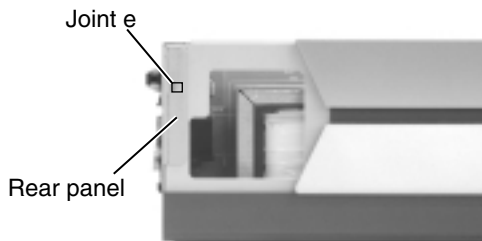


Fig.12

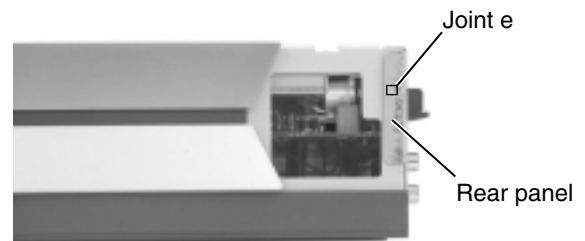
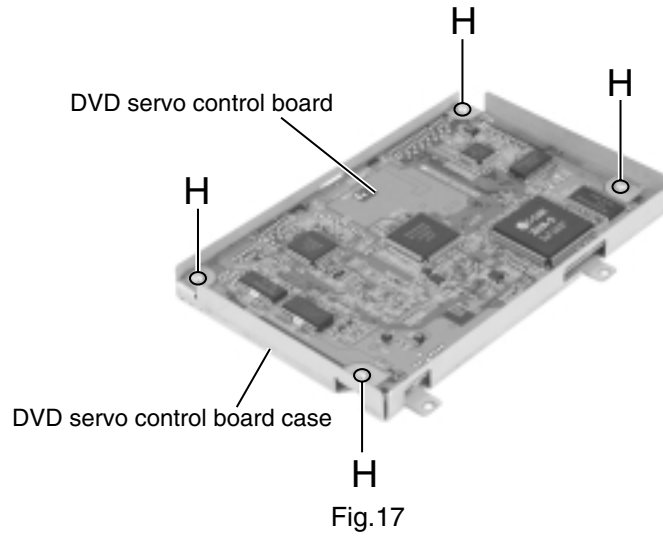
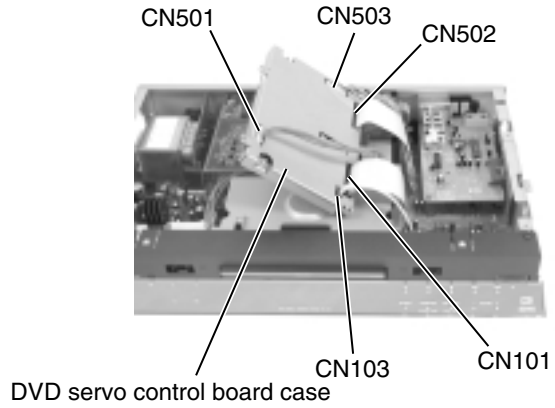
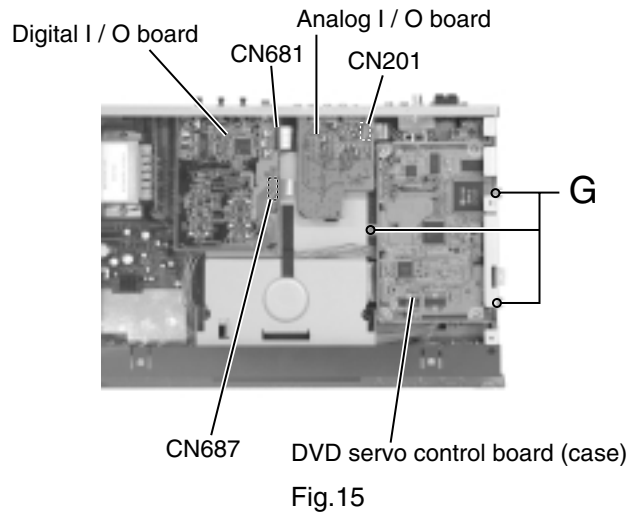


Fig.12

**■Removing the DVD servo control board
(See Fig.15 to 17)**

- Prior to performing the following procedure, remove the right side cover, the top cover, and the rear cover.
1. Remove the three screws G and pull the DVD servo control board case upward.
 2. Disconnect the harness from connector CN501 and CN503, and the card wire from CN101, CN103 and CN502 of the DVD servo control board on the underside of the DVD servo control board case.
 3. Remove the four screws H attaching the DVD servo control board.



■ Removing the analog I / O board / the digital I / O board (See Fig.18 and 19)

- Prior to performing the following procedure, remove the top cover and the rear cover.
1. Remove the two screws E attaching the analog I / O board on the back of the body.
 2. Disconnect the card wire from connector CN201 on the analog I / O board.
 3. Remove the four screws E attaching the digital I / O board on the back of the body.
 4. Disconnect the card wire from connector CN681 and CN687 on the digital I / O board.

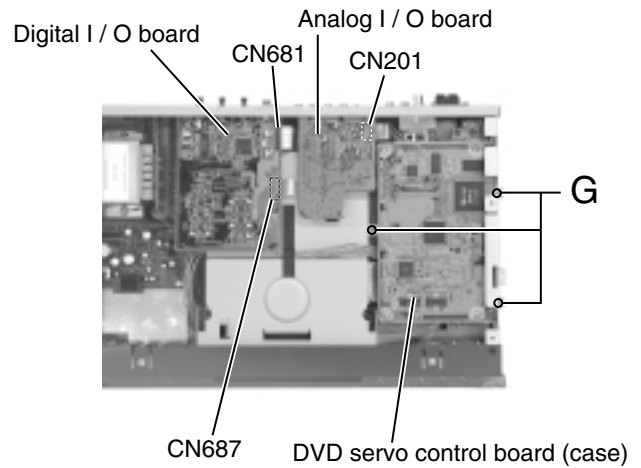


Fig.18

■ Removing the tuner board / the sub board (See Fig.20 and 21)

- Prior to performing the following procedure, remove the top cover, the rear cover and the DVD servo control board case.
1. Remove the two screws E attaching the tuner board on the back of the body.
 2. Disconnect connector CN111 on the tuner board from the sub board.
 3. Disconnect connector CN131 on the sub board from the main board.

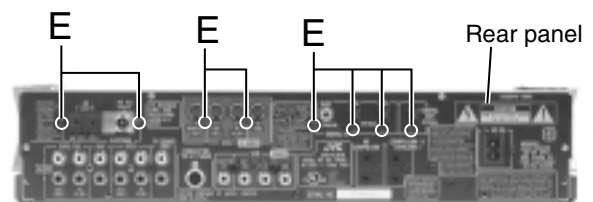


Fig.19

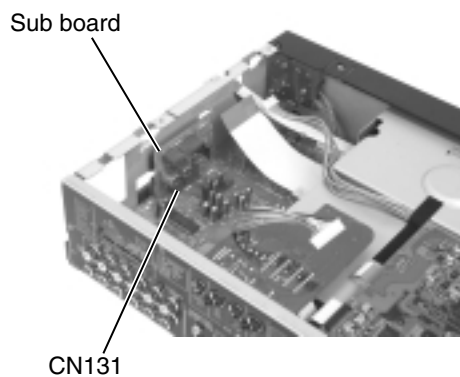


Fig.21

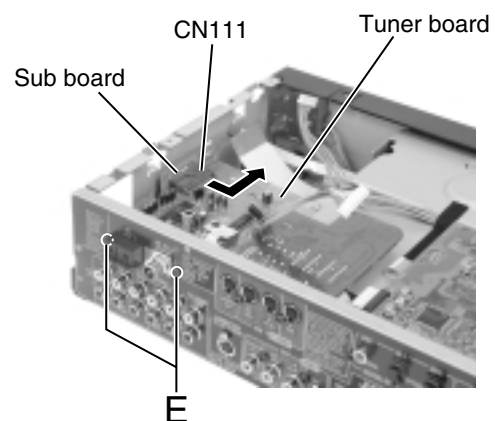


Fig.20

■Removing the DVD mechanism assembly
(See Fig.22 and 23)

- Prior to performing the following procedure, remove the top cover, the rear cover, the front panel assembly, the DVD servo control board case, the analog I / O board, the digital I / O board and the tuner board.
1. Disconnect the harnesses from the spacer on the upper side of the DVD mechanism cover.
 2. Remove the two screws I and the one screw J attaching the DVD mechanism cover.
 3. Remove the two screws K attaching the DVD mechanism assembly.
 4. Remove the DVD mechanism assembly upward while pulling it backward.

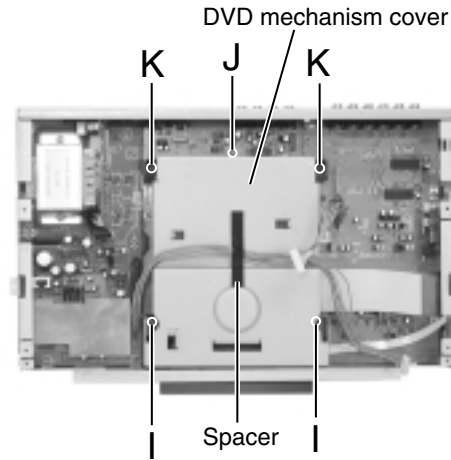


Fig.22

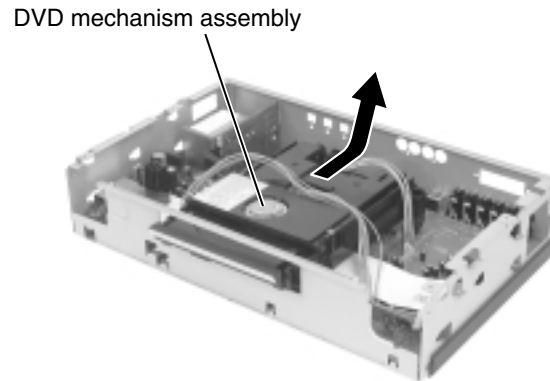


Fig.23

■Removing the power board
(See Fig.24 and 25)

- Prior to performing the following procedure, remove the top cover, the rear cover, the front panel assembly, the DVD servo control board case and the digital I / O board.
1. Disconnect the harness from the spacer on the upper side of the DVD mechanism cover.
 2. Remove the two screws E attaching the power board on the back of the body.
 3. Disconnect the harness from connector CN911 and CN912 on the power board.
 4. Remove the four screws L attaching the power board.
 5. Disconnect connector CN913 and CN914 of the power board from the main board by pulling out them respectively.

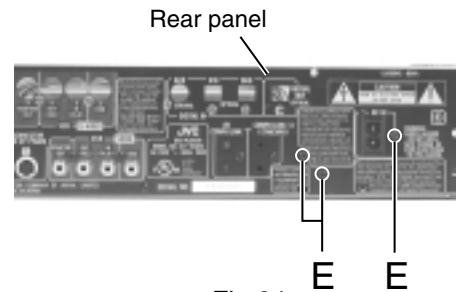


Fig.24

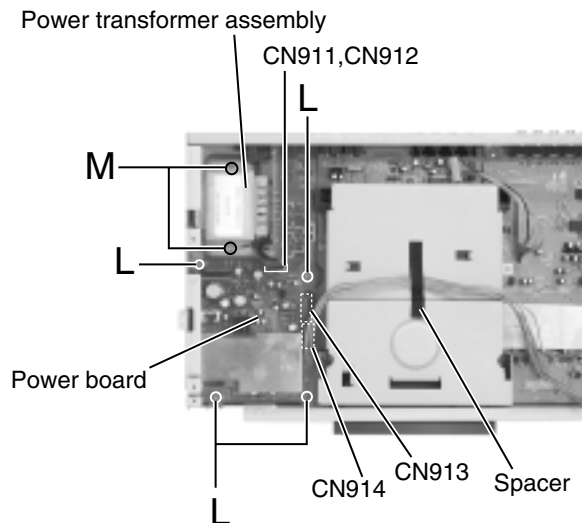


Fig.25

■ Removing the power transformer assembly (See Fig.24 and 25)

• Prior to performing the following procedures, remove the top cover and the rear cover.

1. Disconnect the harnesses from connector CN911 and CN912 on the power board.
2. Remove the two screws M attaching the power transformer assembly.
3. Remove the screw E attaching the power transformer assembly on the back of the body.

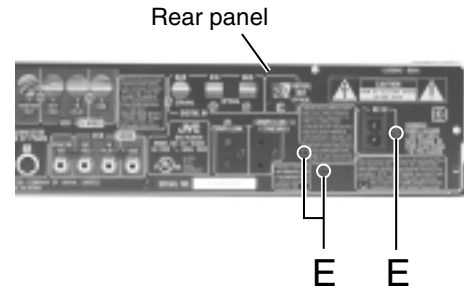


Fig.24

■ Removing the main board (See Fig.26)

• Prior to performing the following procedure, remove the top cover, the rear cover, the front panel assembly, the rear panel, the DVD mechanism assembly, the power board and the sub board.

1. Remove the four DVD spacers on the upper side of the main board.
2. Remove the five screws N attaching the main board.

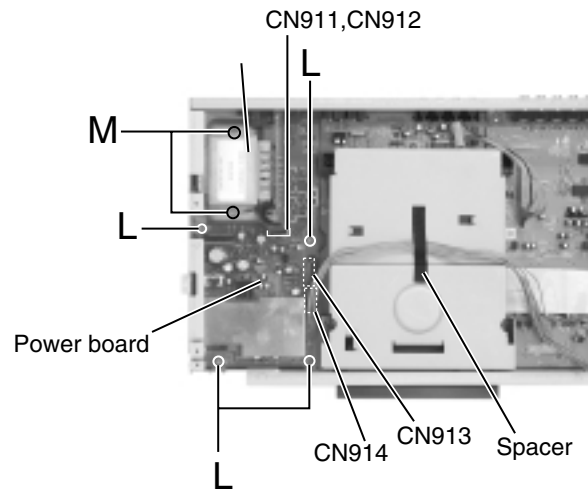


Fig.25

<Front panel assembly>

• Prior to performing the following procedure, remove the top cover, the rear cover, the side covers and the front panel assembly.

■ Removing the power switch board (See Fig.27)

1. Disconnect the harness from connector CN705 on the power switch board.
2. Remove the three screws O attaching the power switch board.

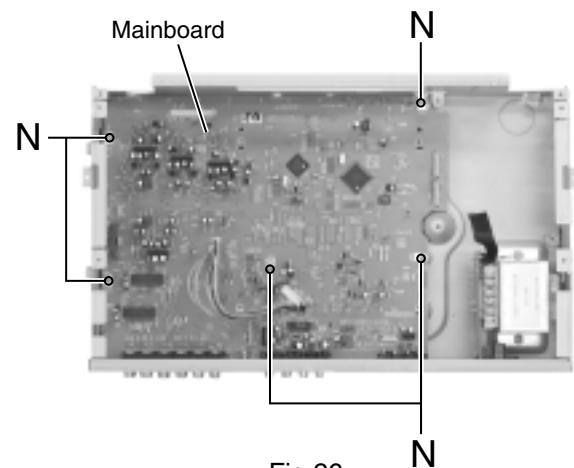


Fig.26

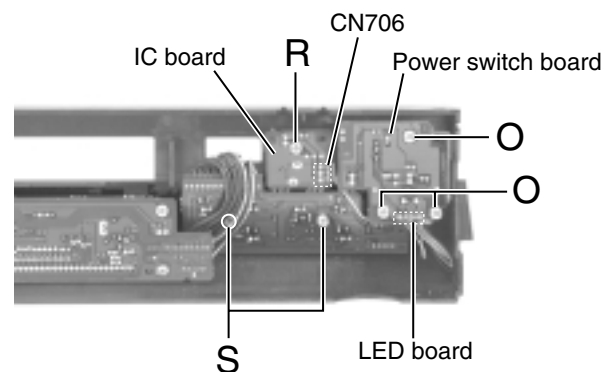


Fig.27

■Removing the eject board (See Fig.28)

1. Disconnect the harness from connector CN702 on the eject board.
2. Remove the three screws P attaching the eject board.

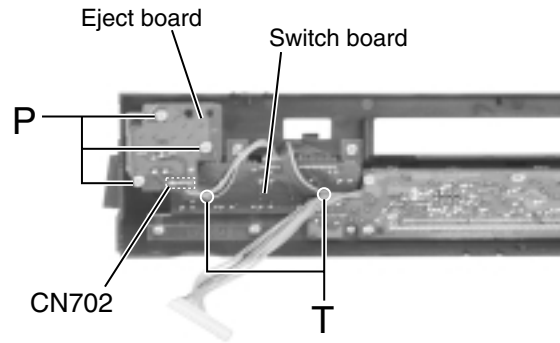


Fig.28

■Removing the LCD board (See Fig.29)

1. Remove the four screws Q attaching the LCD board.
2. Unsolder WA701, WA703 and WA704 on the LCD board.

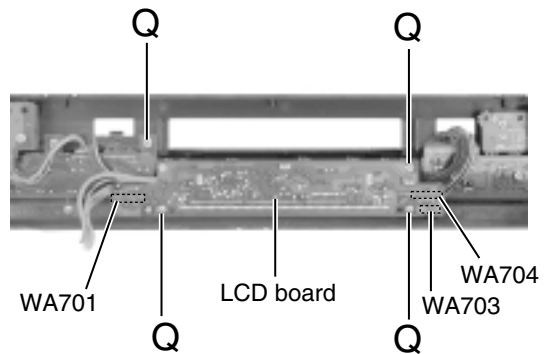


Fig.29

■Removing the IC board (See Fig.27)

1. Remove the screw R attaching the IC board.
2. Disconnect the harness from connector CN706 on the IC board.

■Removing the LED board (See Fig.27)

- Prior to performing the following procedure, remove the LCD board and the IC board.

1. Disconnect the harness from connector CN705 on the power switch board.
2. Remove the two screws S attaching the LED board.

■Removing the switch board (See Fig.28)

- Prior to performing the following procedure, remove the LCD board.

1. Disconnect the harness from connector CN702 on the eject board.
2. Remove the two screws T attaching the switch board.

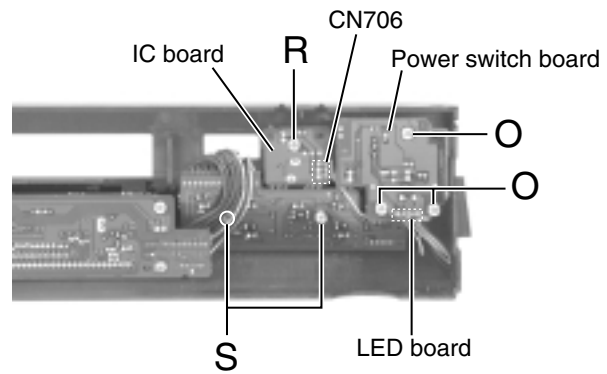


Fig.27

<Removing DVD mechanism unit>

■ Removing the clamper base (refer to Figure 1)

- o Remove the top cover.
 - o Remove the DVD mechanism unit.
1. Remove the two screws at A fixing the clamper base.

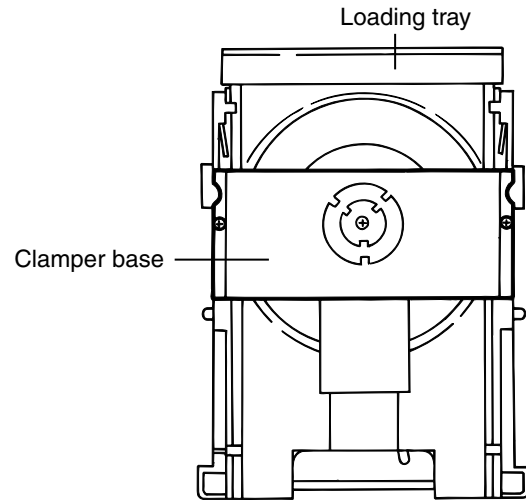


Figure 1

■ Removing the loading tray (refer to Figures 2 - 4)

- o Remove the clamper base.
1. Turn the up-down cam lever clockwise (in the direction of the arrow in Figure 2) to lower the position of the mechanism.
 2. Manually set the loading tray to the fully-open position.
 3. Stretch the tray stoppers on both sides of the loading base outward and pull out the tray.

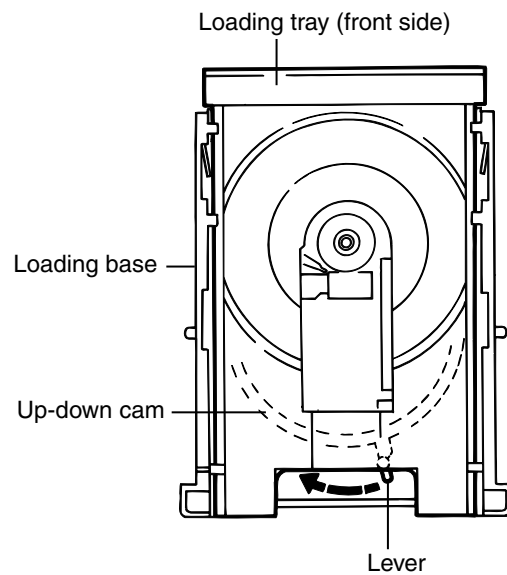


Figure 2

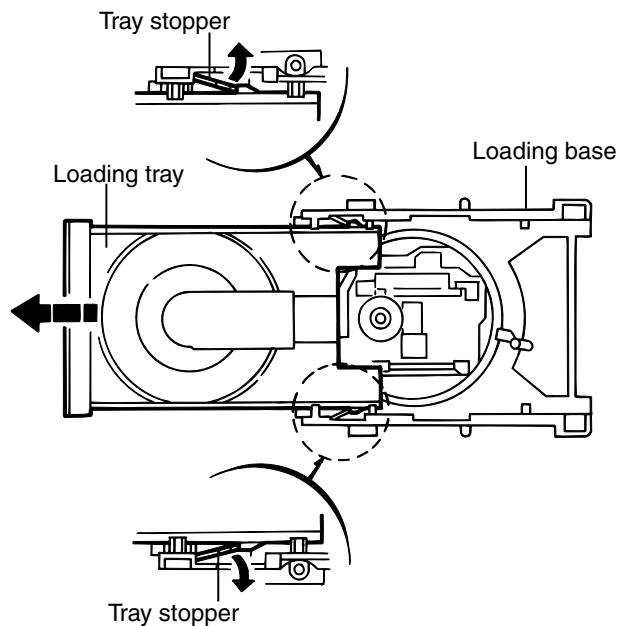


Figure 4

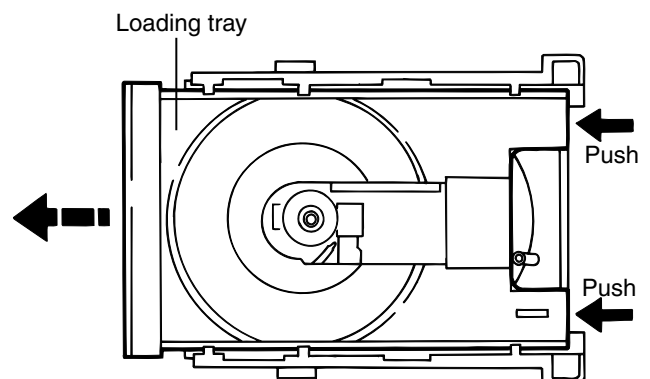


Figure 3

■ **Removing the traverse mechanism unit** (refer to Figure 5)

- o Remove the loading tray.
- 1. Remove the three screws at B fixing the traverse mechanism unit.

■ **Protecting the optical pickup**

- o Solder the flexible ground point on the optical pickup when replacing the pickup or before detaching the mechanism control board. When assembling the unit, remove the solder last.

■ **Removing the mechanism control board**

(refer to Figures 6 - 7)

- o Remove the traverse unit. (Can be detached without detaching the T-mechanism unit.)
- 1. Remove the two screws at C fixing the mechanism control base from the bottom of the traverse unit.
- 2. Pull out the CN12 connector and detach the mechanism control board.
- 3. Remove the card wire from the CN13 connector on the mechanism control board.
- 4. Pull out the FPC holder from the CN12 connector on the reverse side of the mechanism control board and remove the flexible harness, referring to Figure 7.

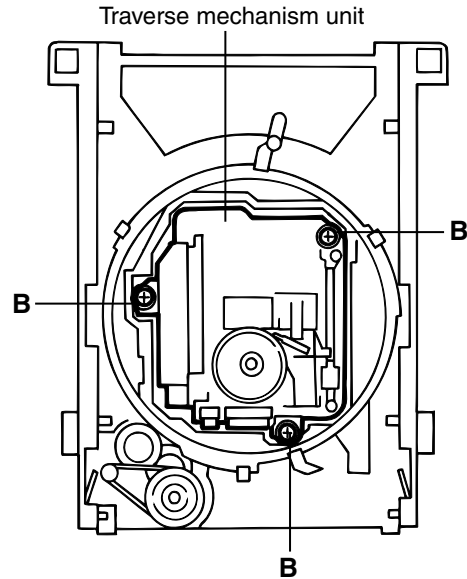


Figure 5

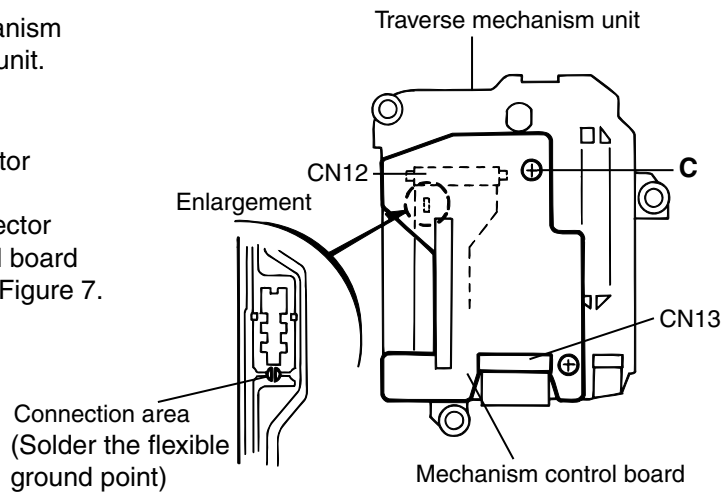


Figure 6

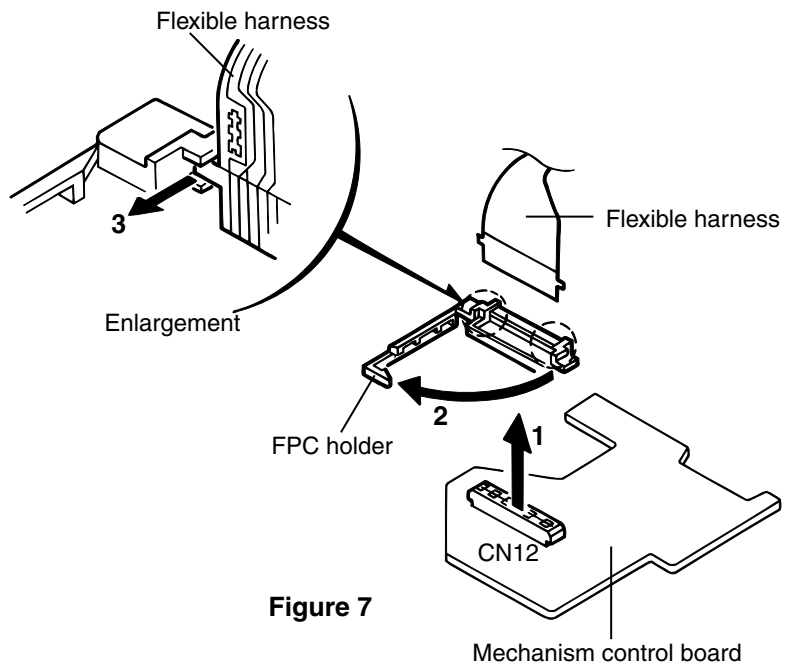


Figure 7

■ Removing the turntable and spindle motor assembly

(refer to Figures 8 - 9)

- o Remove the traverse mechanism unit.
 - o Solder the flexible ground point on the optical pickup. (Figure 6)
 - o Remove the mechanism control board.
1. Remove the flexible harness from the feed motor connector on the spindle motor board assembly.
 2. Remove the three screws at D fixing the spindle motor from the bottom of the traverse chassis.

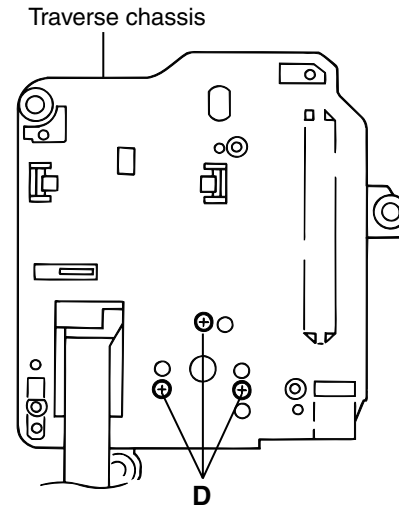


Figure 8

■ Removing the feed motor unit (refer to Figure 9)

- o Remove the traverse mechanism unit.
 - o Remove the mechanism control board.
1. Remove the FPC from the feed motor connector on the turntable spindle motor board.
 2. Remove the two screws at E fixing the feed motor unit.

■ Removing the optical pickup unit (refer to Figure 9)

- o Remove the traverse mechanism unit.
 - o Remove the mechanism control board.
 - o Remove the feed motor unit.
1. Remove the screw at F fixing the guide shaft holder at B, then simultaneously remove the guide shaft at B and the optical pickup unit. While doing so, slide the unit horizontally away from the guide shaft at A.

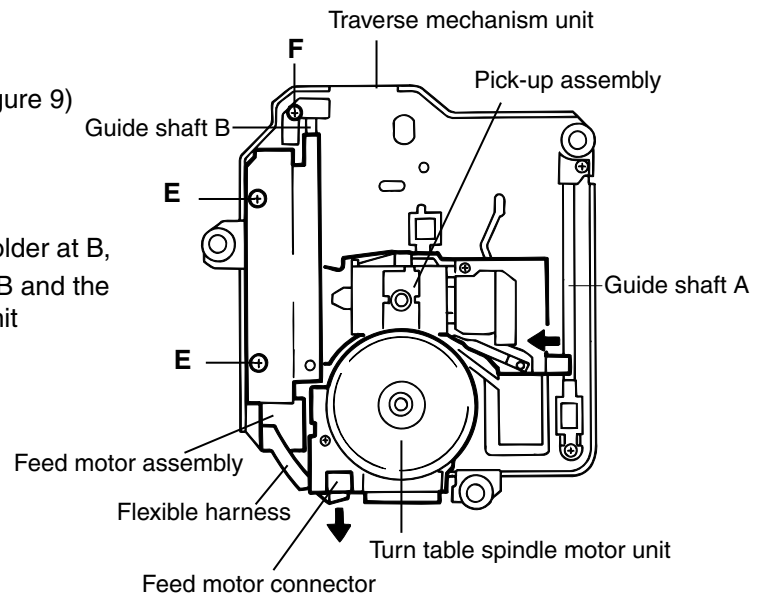


Figure 9

■ **Removing the loading mechanism parts**

(refer to Figures 10 - 11)

- o Remove the clamper base.
- o Remove the disk tray.
- 1. Turn the lever counterclockwise until it stops (position 1), while pushing the switch lever in the direction of the arrow and pushing up the pawl at A using a screwdriver.
- 2. Stretch the two pawls at B outward using a screwdriver and remove the chassis.
- 3. Turn the lever clockwise (position 2) to remove the up-down cam.
- 4. Remove the pulley gear and the pulley gear belt after removing the screw at G fixing the pulley gear.
- 5. Pull out drive gear 2 then drive gear 1.

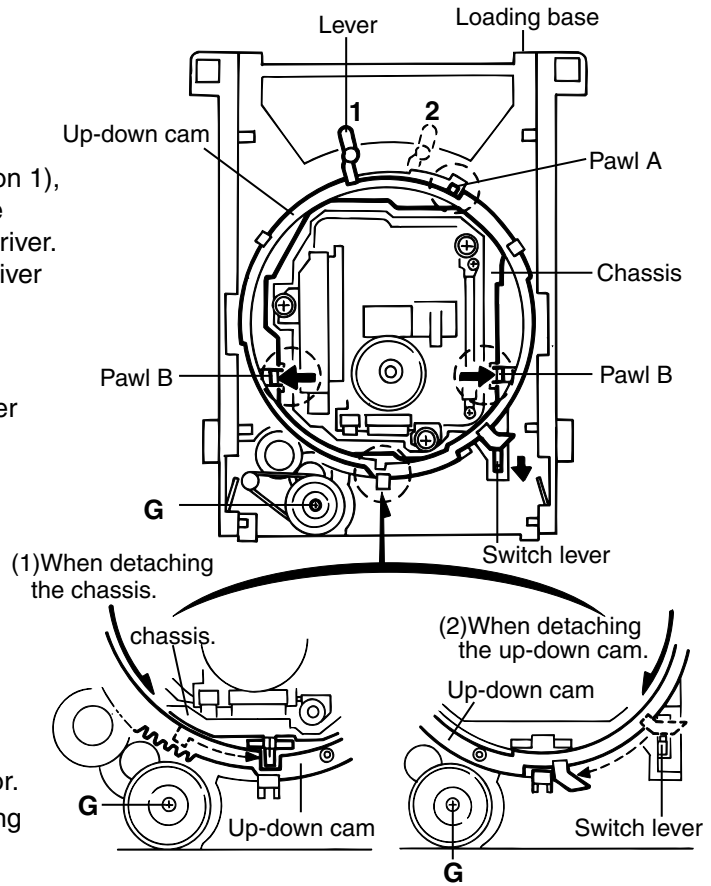


Figure 10

■ **Removing the loading motor board**

(refer to Figures 11 - 12)

- o Remove the clamper base.
- o Remove the disk tray.
- 1. Remove the loading belt.
- 2. Remove the two screws at H fixing the loading motor.
- 3. Remove the screw at I and the three pawls at C fixing the loading motor base from the reverse side of the loading base.

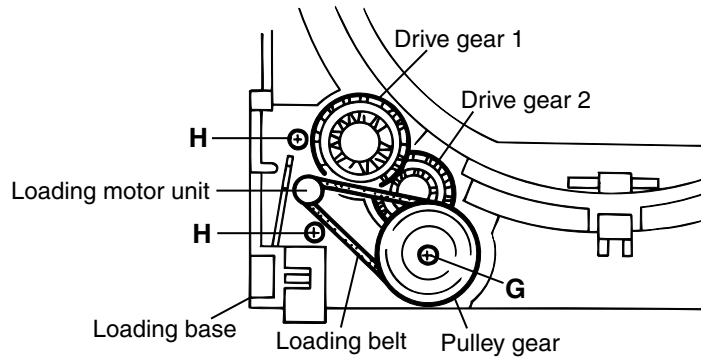


Figure 11

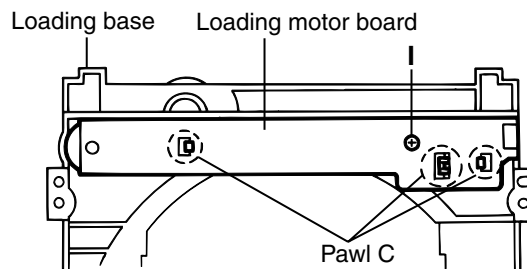


Figure 12

Disassembly method

<Speaker>

■ Removing the amplifier assembly (See Fig.1)

1. Remove the twelve screws A attaching the amplifier assembly on the back of the body.
2. Move the amplifier assembly backward and disconnect the harness from connector CN109 in the lower part of the amplifier assembly.

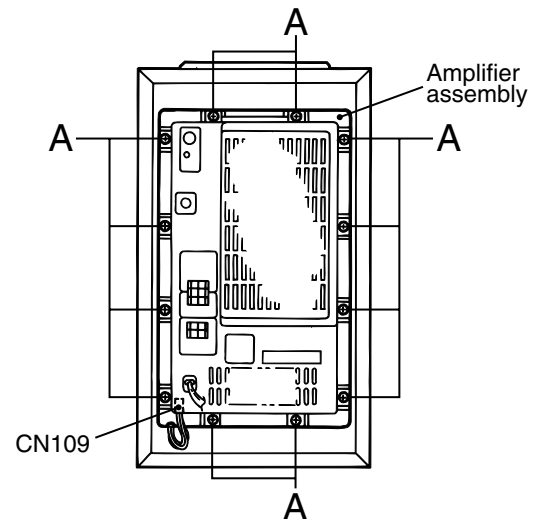


Fig.1

■ Removing the heat sink cover and the amplifier cover (See Fig.2 and 3)

- Prior to performing the following procedure, remove the amplifier assembly.

1. Pull out the volume knob.
2. Remove the four screws B attaching the heat sink cover.
3. Remove the twenty screws C and the one screw D attaching the amplifier cover.

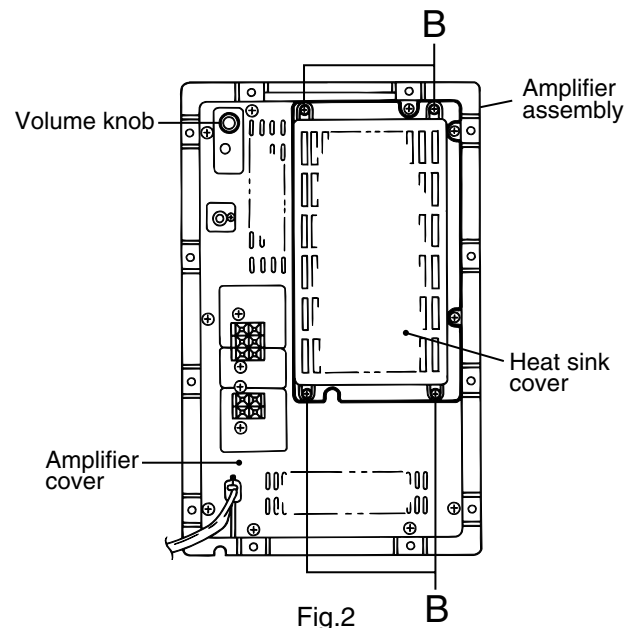


Fig.2

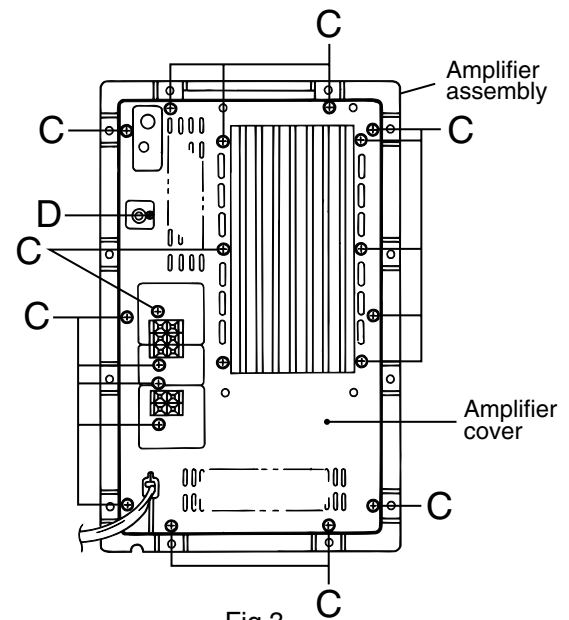


Fig.3

■ Removing the front panel assembly (See Fig. 6 to 9)

- Prior to performing the following procedure, remove the top cover, the rear cover and the side covers.
1. Disconnect the harness from connector CN802 on the main board on the upper side of the body.
 2. Remove the two screws C on the upper side of the body.
 3. Remove the three screws D on the bottom of the body.
 4. Release the five joints c and detach the front panel assembly toward the front.

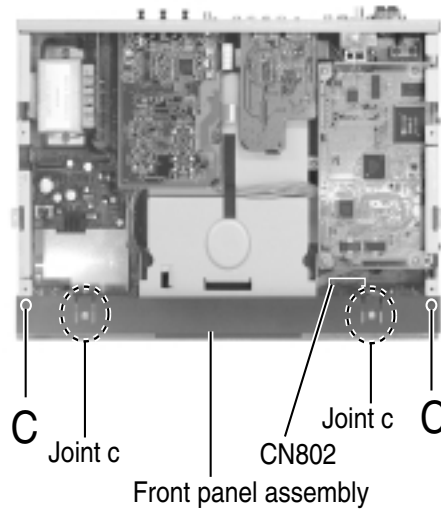


Fig.6

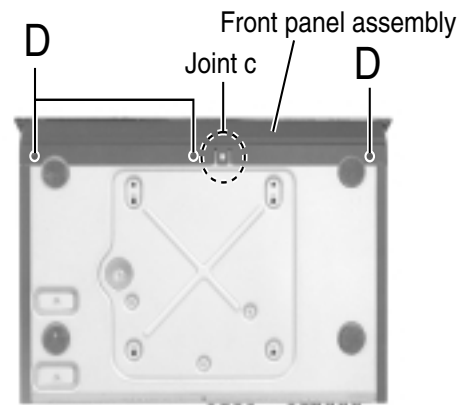


Fig.7

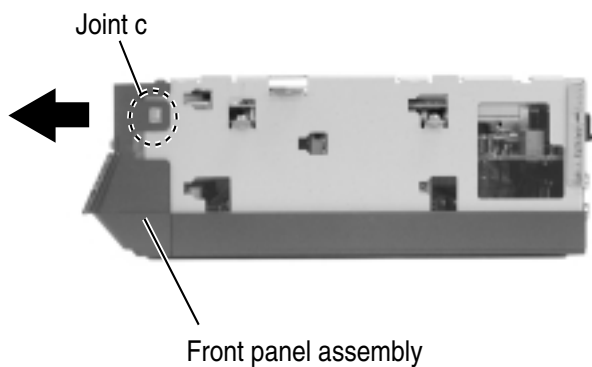


Fig.9

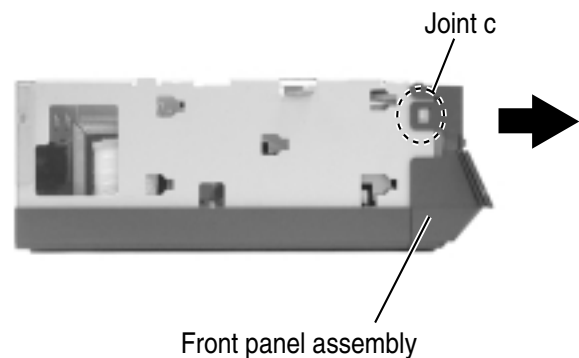


Fig.8

■Removing the right and left corner covers (See Fig.10 and 11)

- Prior to performing the following procedure, remove the top cover, the rear cover, the side covers and the front panel assembly.
 - It is not necessary to remove the front panel assembly.
1. Move the left corner cover backward to release the three joint hooks d.
 2. Remove the right corner cover in the same way.

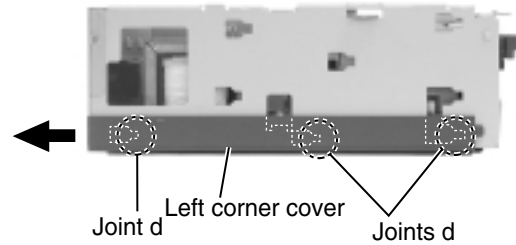


Fig.10

■Removing the rear panel (See Fig.12 to 14)

- Prior to performing the following procedure, remove the top cover and the rear cover.
1. Remove the eighteen screws E and the one screw F attaching the rear panel.
 2. Release the two joints e on both sides of the body.

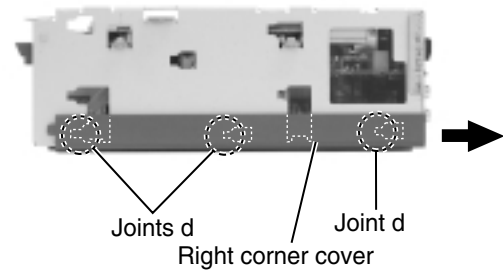


Fig.11

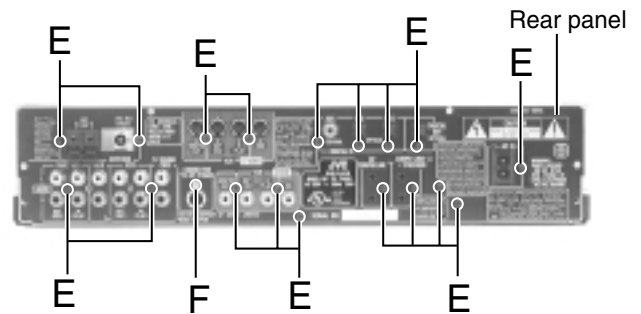


Fig.12

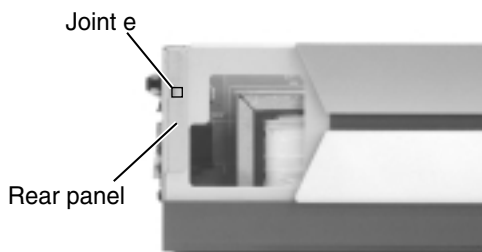


Fig.12

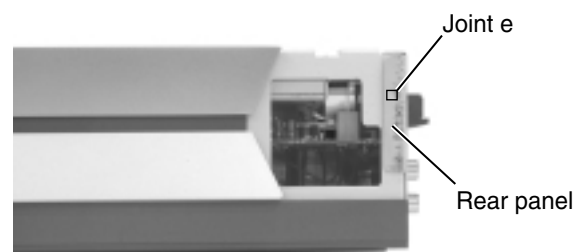


Fig.12

**■Removing the DVD servo control board
(See Fig.15 to 17)**

- Prior to performing the following procedure, remove the top cover, the rear cover and the right side cover.
1. Remove the three screws G and pull the DVD servo control board case upward.
 2. Disconnect the harness from connector CN501 and CN503, and the card wire from CN101, CN103 and CN502 of the DVD servo control board on the underside of the DVD servo control board case.
 3. Remove the four screws H attaching the DVD servo control board.

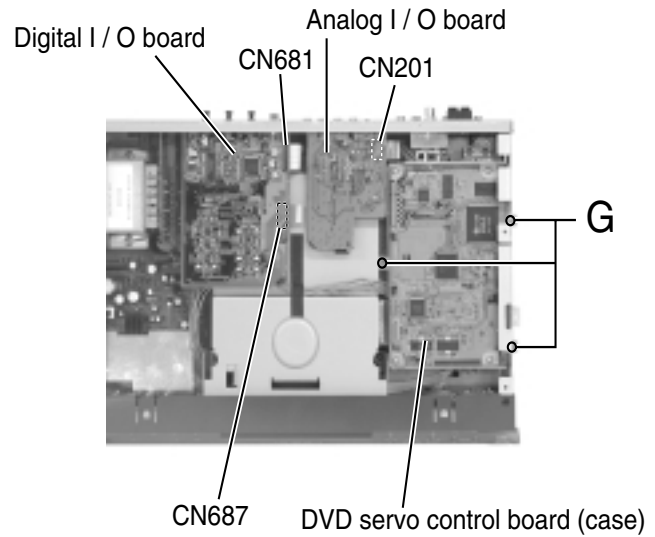


Fig.15

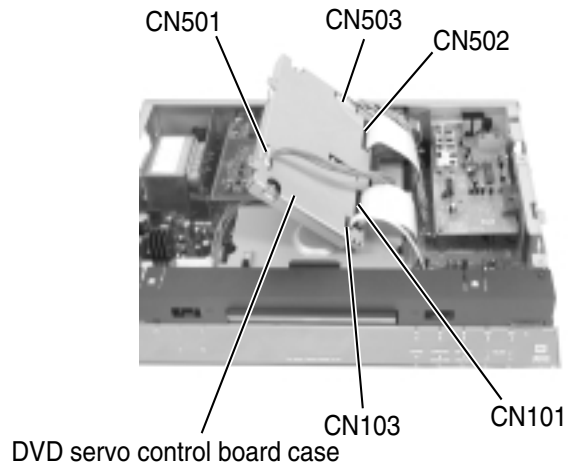


Fig.16

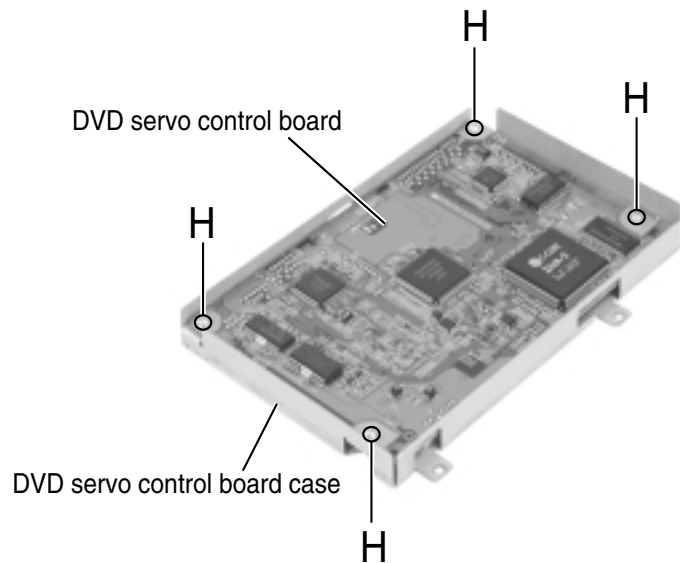


Fig.17

Main Adjustment

Adjustment and confirmation matter

(1) Auto adjustment method

If microprocessor (IC401, IC402, IC714, IC716) or DVD Prek-up is replaced, initialize the DVD player in the following matter:

1. Initialize the DVD player in the following matter:

- 1) Make sure that no disc is on the tray.
- 2) Insert the power pulag to the outlet while pressing "PLAY" and "OPEN/CLOSE" button at the same time.
FL Display indicate ¥ ; Region cord.
- 3) Press Enter button. And EEPROM initialize start.
- 4) When indicate "96kHz EEPROM" on the display , initialize finished.

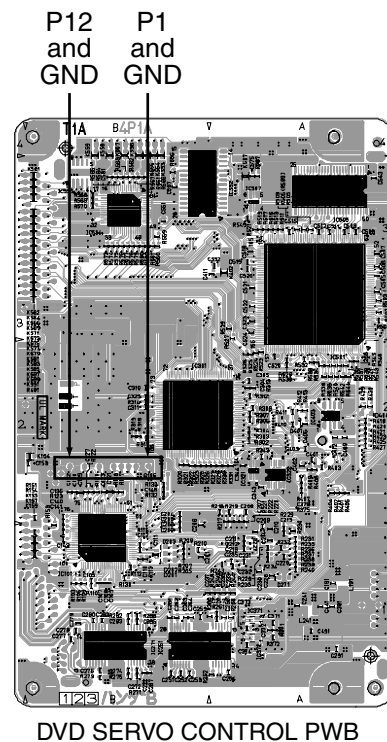
Note : During the EEPROM initialization the keys may not be operated.
Press the "POWER" key to initiate the STAND-BY mode and the test mode will then be cancelled.

(2) Confirmation of DVD RF level

- 1.The oscilloscope is connected between "1"(RFOP) of CN104 and "2"(GND).
- 2.Reproduction of the test disc (VT-501) made by JVC.
- 3.It is confirmed that RF LEVEL is $350\text{mVp-p} \pm 150\text{mVp-p}$.
- 4.When there is disorder in the waveform road cuts etc, test disk is exchanged and measured.

(3) Confirmation of CD jitter level and RF level

1. The CD jitter meter is connected between "11"(GND) of CN104 and "12"(FLTOUT).
The RF level is observed at the same time.
- 2.The first test disk(CTS-1000) made of JVC is reproduced.
- 3.It is confirmed that RF LEVEL is $360 \pm 100\text{mVp-p}$.
5. When there is disorder in the waveform road cuts etc, test disk is exchanged and measured.



FRONT SIDE

(4) Flap adjustment of the Pick-up guide shaft

- 1) Make sure that there is no disc on the tray.
- 2) Press both the "PLAY" and "OPEN/CLOSE" keys of the main unit to activate the primary power and **¥(** ; Version3, ¥; Region cord) will be displayed on the FL indicator.

Note: If the FL indicator display stops and remains at "TEST 0", unplug the power cord from the outlet and after waiting at least 1 second, plug it in again. After the tray open/close procedure has completed, unplug it again and then perform the initialization procedure again.

- 3) Press the "OPEN/CLOSE" key of the main unit to draw the tray out.
*Place the test disk (VT-501) on the tray and then press the "OPEN/CLOSE" key.
(Note: Pushing the tray to close it is not possible.)
- 4) Press the "PLAY" key of the main unit.
- 5) The "JIT 0000" is displayed on the FL indicator.
Set the FL indicator figure value to its minimum by adjusting the pickup guide shaft flap.
* The test mode is cancelled when the power is turned off.

Measurement	Adjustment point	Mode	Disc
—	Refer to Fig.2	Reproduction part	VT-501
Measurement machine	connections	Extension cord No.	
No need	Refer to Fig.1	QUQ110-3740AM	
General tool : Hex-head wrench (1.27 mm)			

"Flap adjustment" of the Pick-up guide shaft adjusts "Tangential adjustment machine screw" A and "Tilt adjustment machine screw" B from the DVD Mechanism A'ssy bottom.

1. The part at the center on the DVD test disc is reproduced.
2. The flap adjustment screws is turned alternately and adjusted like clearly seeing the waveform of CN104"1" to the way.

Note

1. The tangential adjustment is done finish and, then, tilt is adjusted.
2. The repeat the adjustment 2-3 times, for best result.
3. The final adjustment should be tilt adjustment.

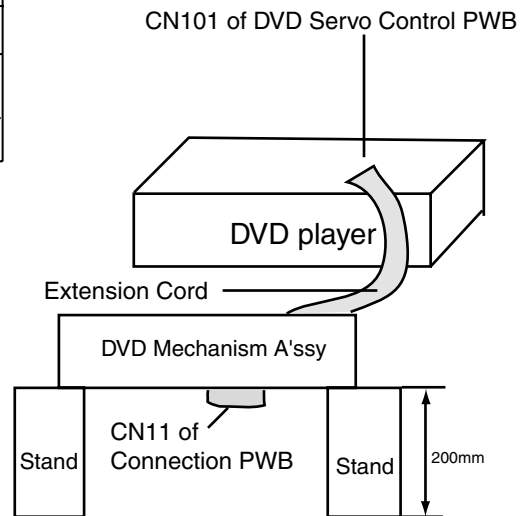


Fig.1

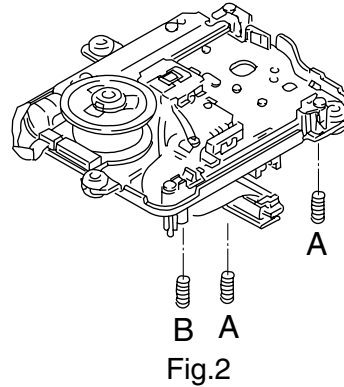


Fig.2

Confirmation after adjustment.

Confirm to reproduce video CD and CD after the DVD test disc is adjusted and to find abnormality.

(5) About keeping the disc

As for the DVD test disc, plane accuracy is demanded. Please note the keeping place on the disc.

1. Please do not put the disc directly on the work desk etc. after uses .
2. To keep the planarity of the disc, politely handle ,and please put in a special case and keep the disc vertically after uses .
Please keep keeping the disc in a cool place where direct sunshine and the air-conditioning wind do not drive.
3. When the disc curves,an accurate adjustment cannot be done.
Please exchange for a new test disc and adjust optics.
4. Other discs might not be able to be reproduced when adjusting on a curved disc.

Point of adjustment

- * Please execute the static electricity protection measures before starting the adjustment.
- * When the following parts are exchanged,optical adjustment "Adjust the flap of the disc motor" is necessary.
 - 1.The disc motor was exchanged.
 - 2.The laser pick up was exchanged.
 - 3.The traverse motor unit was exchanged.

Note

Additionally, please adjust the flap of the disc motor when the picture quality deterioration is seen .The basic adjustment though, is unnecessary for part exchange in the traverse.

An optical adjustment in the laser pick up cannot be done.

Please adjust the flap of the disc motor after exchanging the laser pick up.

- * When the traverse unit is exchanged, the adjustment is basically unnecessary.

Precautions for Service

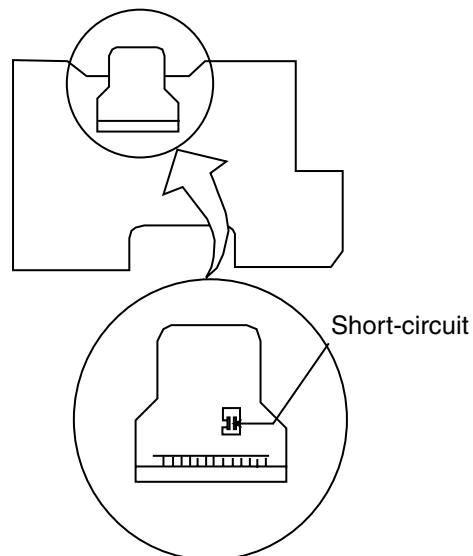
Handling of Traverse Unit and Laser Pickup

1. Do not touch any peripheral element of the pickup or the actuator.
2. The traverse unit and the pickup are precision devices and therefore must not be subjected to strong shock.
3. Do not use a tester to examine the laser diode. (The diode can easily be destroyed by the internal power supply of the tester.)
4. To replace the traverse unit, pull out the metal short pin for protection from charging.
5. When replacing the pickup, after mounting a new pickup, remove the solder on the short land which is provided at the center of the flexible wire to open the circuit.
6. Half-fixed resistors for laser power adjustment are adjusted in pairs at shipment to match the characteristics of the optical block.
Do not change the setting of these half-fixed resistors for laser power adjustment.

Destruction of Traverse Unit and Laser Pickup by Static Electricity

Laser diodes are easily destroyed by static electricity charged on clothing or the human body. Before repairing peripheral elements of the traverse unit or pickup, be sure to take the following electrostatic protection:

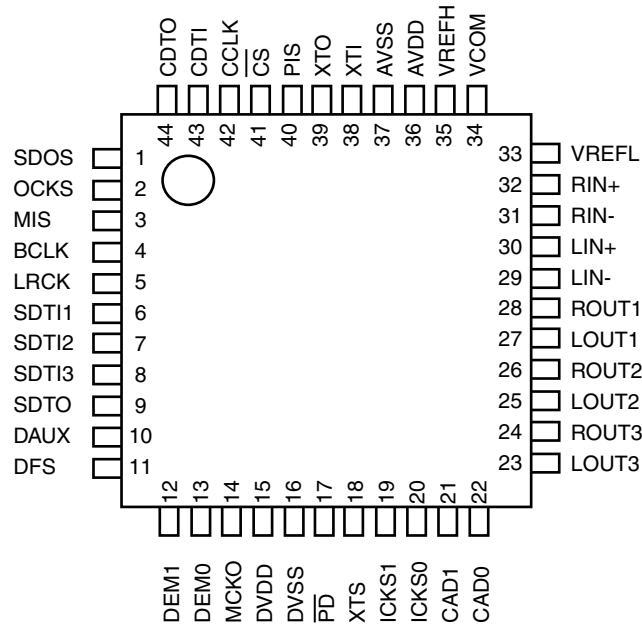
1. Wear an antistatic wrist wrap.
2. With a conductive sheet or a steel plate on the workbench on which the traverse unit or the pick up is to be repaired, ground the sheet or the plate.
3. After removing the flexible wire from the connector (CN101), short-circuit the flexible wire by the metal clip.
4. Short-circuit the laser diode by soldering the land which is provided at the center of the flexible wire for the pickup.
After completing the repair, remove the solder to open the circuit.



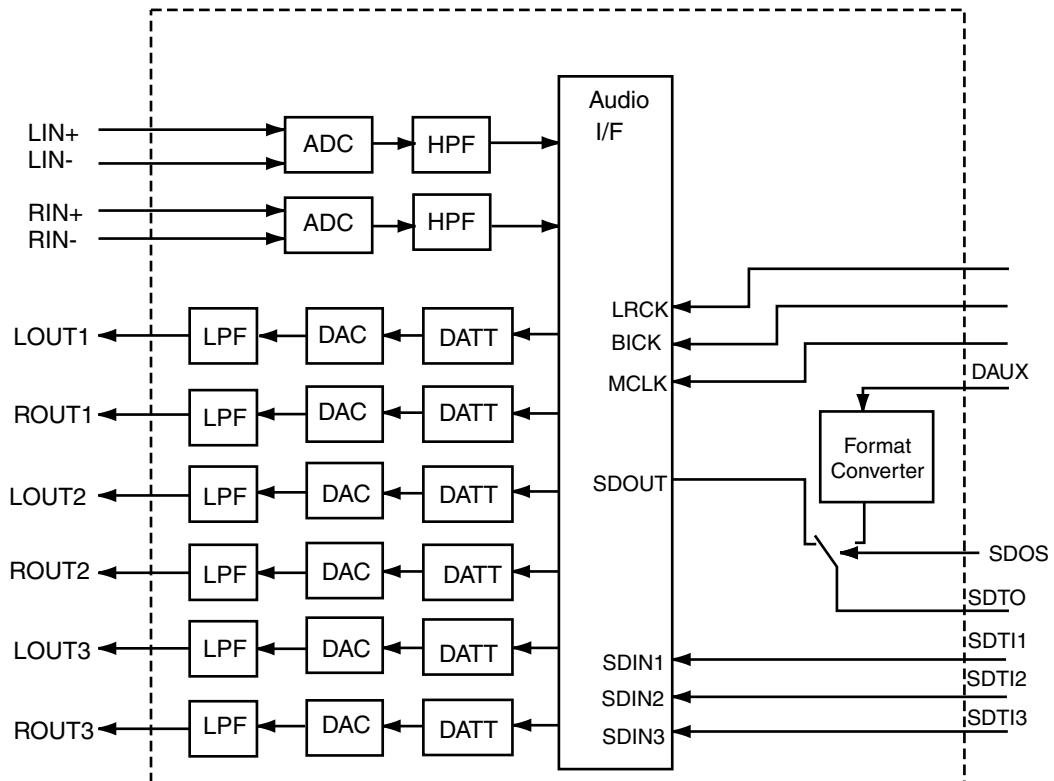
Discription of major IC's

■ AL4527 (IC601): A/D, D/A Converters

1. Terminal layout



2. Block diagram

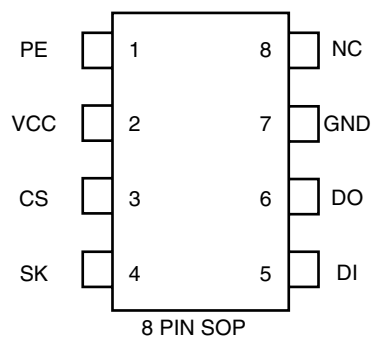


3. Pin function

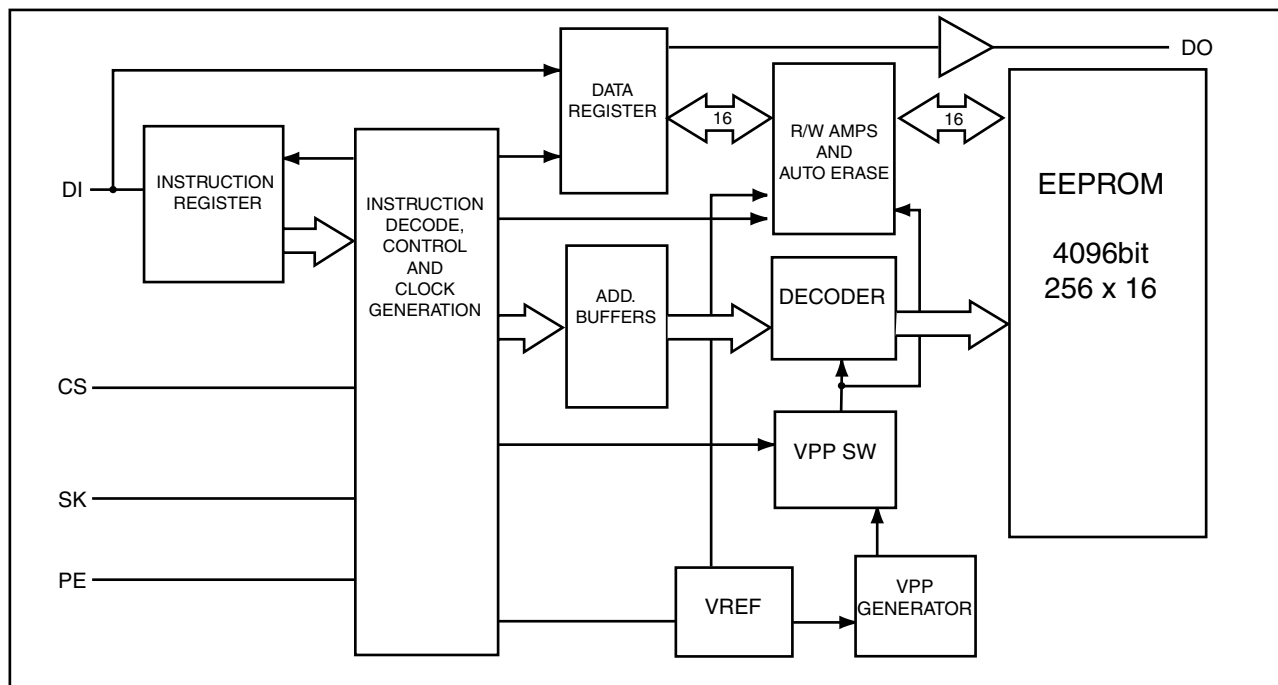
Pin No.	Symbol	I/O	Functions
1	SDOS	I	SDTO source select terminal L: Internal ADC output H: DAUX input
2	OCKS	I	Serial control mode select terminal L: 3-wire serial H: IC bus
3	MIS	I	Soft mute terminal H: Starting Soft mute L: Cancel
4	BCLK	I	Audio serial data clock terminal
5	LRCK	I/O	Input channel clock terminal
6	SDTI1	I	DAC1 audio serial data input terminal
7	SDTI2	I	DAC2 audio serial data input terminal
8	SDTI3	I	DAC3 audio serial data input terminal
9	SDTO	O	Audio serial data output terminal
10	DAUX	I	Auxiliary audio serial data input terminal
11	DFS	I	2x sampling mode terminal L: Ordinal speed H: 2x speed
12	DEM1	I	De-emphasize 1 terminal
13	DEM0	I	De-emphasize 2 terminal
14	MCKO	-	Power terminal for output buffer 2.7 5.5 V
15	DVDD	-	Digital power supply terminal 4.5 5.5 V
16	DVSS	-	Digital ground terminal 0 V
17	PD	I	Power down & reset terminal L: Power is down and register is initialized.
18	XTS	I	Input clock selection 2 terminals
19	ICKS1	I	Input clock selection 1 terminals
20	ICKS0	I	Input clock selection 0 terminals
21	CAD1	I	Chip address 1 terminal
22	CAD0	I	Chip address 0 terminal
23	LOUT3	O	DAC3 L channel analog output terminal
24	ROUT3	O	DAC3 R channel analog output terminal
25	LOUT2	O	DAC2 L channel analog output terminal
26	ROUT2	O	DAC2 R channel analog output terminal
27	LOUT1	O	DAC1 L channel analog output terminal
28	ROUT1	O	DAC1 R channel analog output terminal
29	LIN-	I	L channel analog reverse input terminal
30	LIN+	I	L channel analog non-reverse input terminal
31	RIN-	I	R channel analog reverse input terminal
32	RIN+	I	R channel analog non-reverse input terminal
33	VREF	O	Zero input detection terminal L: P/S = H
34	VCOM	O	COMMON voltage output terminal
35	VREFH	-	Reference voltage input terminal
36	AVDD	-	Analog power supply terminal 4.5 5.5 V
37	AVSS	-	Analog ground terminal 0 V
38	XTI	O	Zero input detection terminal L: P/S = H
39	XTO	I	Master clock input terminal
40	PIS	I	Parallel/serial select terminal L: Serial control mode H: Parallel control mode
41	CS	I I	Audio data interface format 0 terminal (with parallel control mode) Chip select terminal (with 3-wire serial control mode)
42	CCLK	I I	Audio data interface format 0 terminal (with parallel control mode) Control data clock terminal (with serial control mode)
43	CDTI	I I/O	Loopback mode 0 terminal (with parallel control mode) Control data input terminal (with serial control mode)
44	CDTO	I	Loopback mode 1 terminal

■ AK93C65AF-X (IC403) : EEPROM

1. Terminal layout



2. Block diagram



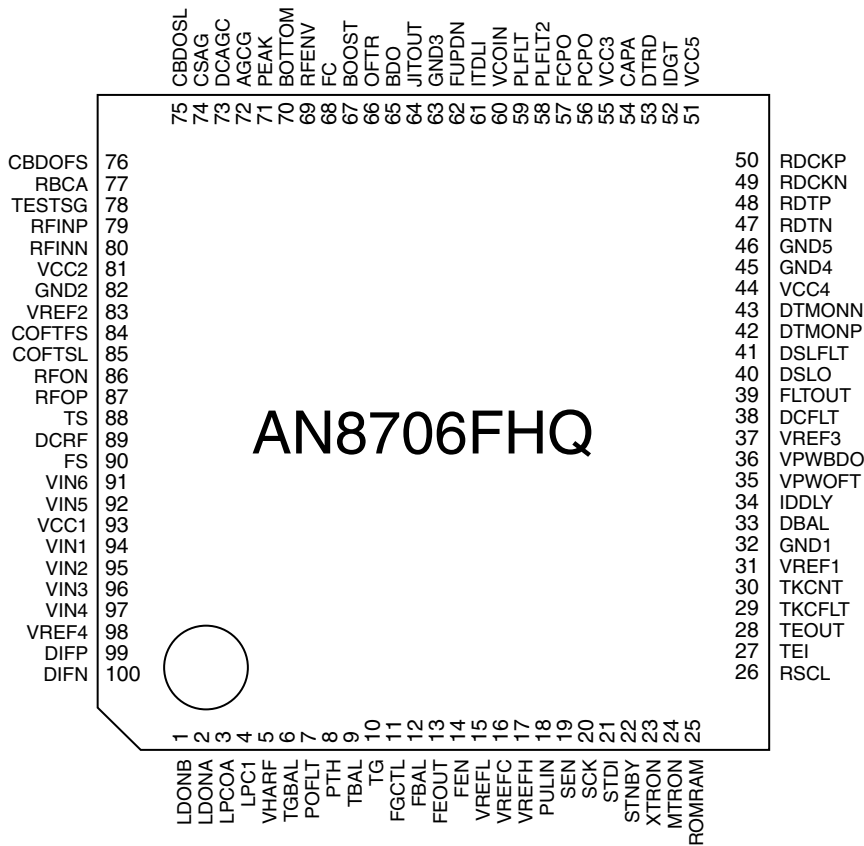
3. Pin function

Pin no.	Symbol	Function
1	PE	Program enable (With built-in pull-up resistor)
2	VCC	Power supply
3	CS	Chip selection
4	SK	Cereal clock input
5	DI	Cereal data input
6	DO	Cereal data output
7	GND	Ground
8	NC	No connection

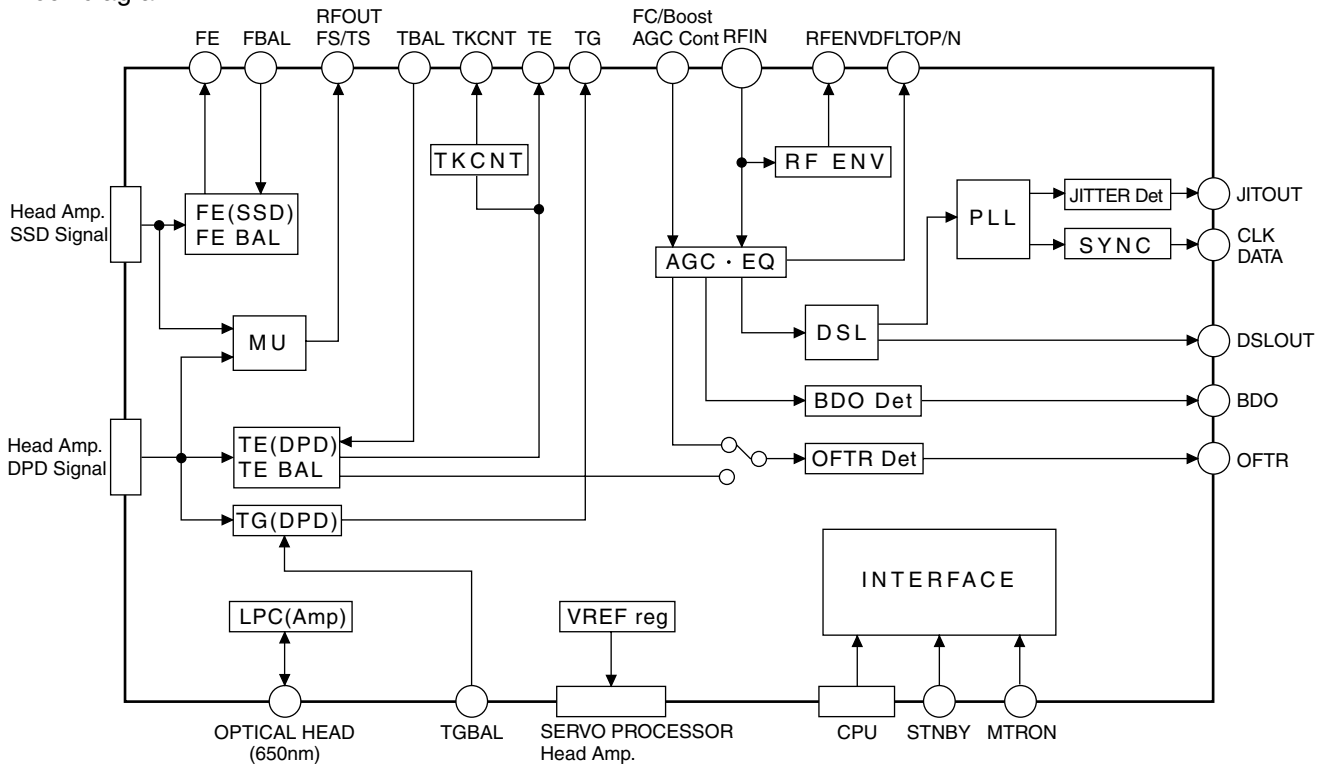
NOTE : The pull-up resistor of the PE pin is about 2.5M Ω (VCC=5V)

■ AN8706FHQ (IC101) : Front end processor

1.Pin layout



2.Block diagram



3.Pin function

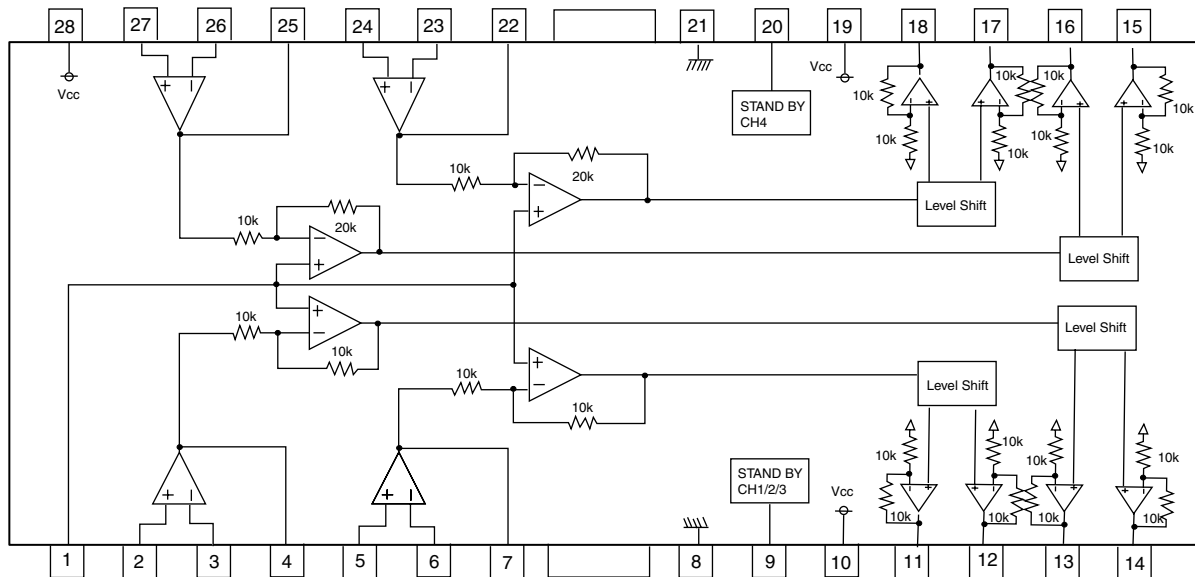
AN8706FHQ (1/2)

Pin No.	Symbol	I/O	Functions
1	LDONB	I	Laser ON (CD Head) terminal
2	LDONA	I	Laser ON (DVD Head) terminal
3	LPCOA	O	Laser drive output terminal
4	LPC1	I	Laser PIN input terminal
5	VHARF	O	VHALF voltage output terminal
6	TGBAL	I	Tangential phase balance control terminal
7	POFLT	O	Track detection Threshold value level terminal
8	PTH	I	Track detection Threshold value level terminal
9	TBAL	I	Tracking balance control terminal
10	TG	O	Tangential phase error signal output terminal
11	FGCTL	I	Focus amplifier Gain control terminal
12	FBAL	I	Focus balance control terminal
13	FEOUT	O	Focus error signal output terminal
14	FEN	I	Focus error output amplifier reversing input terminal
15	VREFL	O	VREFL voltage output terminal
16	VREFC	O	VREFC voltage output terminal
17	VREFH	O	VREFH voltage output terminal
18	PULIN	I	DSL,PLL drawing mode switch terminal
19	SEN	I	SEN(Cereal data input terminal)
20	SCK	I	SCK(Cereal data input terminal)
21	STDI	I	STDI(Cereal data input terminal)
22	STNBY	I	Standby mode control terminal
23	XTRON	I	Tracking OFF holding input terminal
24	MTRON	I	Monitor output ON/OFF switch terminal
25	ROMRAM	I	ROM · RAM switch terminal
26	RSCL	O	Standard current source terminal
27	TEI	I	Tracking error output Amp reversing input terminal
28	TEOUT	O	Tracking error signal output terminal
29	TKCFLT	O	Track count detection filter terminal
30	TKCNT	O	Track count output terminal
31	VREF1	O	VREF1 voltage output terminal
32	GND1	O	Earth terminal 1
33	DBAL	I	Data slice offset adjustment terminal
34	IDDLY	I	Data slice delay adjustment terminal
35	VPWOFT	I	OFTR detection level setting terminal
36	VPWBDO	I	BDO detection level setting terminal
37	VREF3	O	VREF3 voltage output terminal
38	DCFLT	O	Capacity connection terminal for data slice input filter
39	FLTOUT	O	Filter amplifier output terminal
40	DSLO	O	Data slice single data output terminal
41	DSLFLT	O	Constant filter terminal when data is sliceddelly
42	DTMONP	O	PLL differential motion 2 making to value edge signal moniter output (+)
43	DTMONN	O	PLL differential motion 2 making to value edge signal moniter output (-)
44	VCC4	I	Power terminal 4 (5V)
45	GND4	O	Earth terminal 4
46	GND5	O	Earth terminal 5
47	RDTN	O	PLL differential motion making to synchronization RF signal reversing output
48	RDTP	O	PLL differential motion making to synchronization RF signal rotation output
49	RDCKN	O	PLL differential motion making synchronization clock reversing output
50	RDCKP	O	PLL differential motion making synchronization clock rotation output

Pin No.	Symbol	I/O	Functions
51	VCC5	I	Power terminal 5 (3.3V)
52	IDGT	I	Data slice part address part gate signal input terminal (For RAM)
53	DTRD	I	Data slice data read signal input terminal(For RAM)
54	CAPA	I	Data slice CAPA(Address)signal input terminal (For RAM)
55	VCC3	I	Power terminal 3 (5V)
56	PCPO	O	PLL phase gain set terminal
57	FCPO	O	PLL frequency gain set terminal
58	PLFLT2	O	PLL low region filter terminal
59	PLFLT	O	PLL high region filter terminal
60	VCOIN	I	PLL VCO input terminal
61	ITDLI	O	PLL jitter free current ripple removal filter terminal
62	FUPDN	I	PLL frequency control input terminal
63	GND3	O	Earth terminal 3
64	JITOUT	O	Detection signal output of jitter
65	BDO	O	BDO output terminal
66	OFTR	O	OFTR output terminal
67	BOOST	I	Booth control terminal for filter
68	FC	I	FC control terminal for filter
69	RFENV	O	RF enve output terminal
70	BOTTOM	O	Bottom enve detection filter terminal
71	PEAK	O	Peak enve detection filter terminal
72	AGCG	O	AGC amplifier gain control terminal
73	DCAGC	O	AGC amp filter terminal
74	CSAG	O	Sag cancellation circuit filter terminal
75	CBDOSL	O	BDO detection capacitor terminal
76	CBDOSF	O	BDO detection capacitor terminal
77	RBCA	O	BCA detection level setting terminal
78	TESTSG	I	TEST signal input terminal
79	RFINP	I	RF signal positive moving input terminal
80	RFINN	I	RF signal reversing input terminal
81	VCC2	I	Power terminal 2 (5V)
82	GND2	O	Earth terminal 2
83	VREF2	O	VREF2 voltage output terminal
84	COFTFS	O	OFTR detection capacitor terminal
85	COFTFL	O	OFTR detection capacitor terminal
86	RFON	O	RF signal output terminal P
87	RFOP	O	RF signal output terminal N
88	TS	O	All addition amplifier (DVD) output terminal
89	DCRF	O	All addition amplifier capacitor terminal
90	FS	O	All addition amplifier (CD) output terminal
91	VIN6	I	Focus input of external division into two terminal
92	VIN5	I	Focus input of external division into two terminal
93	VCC1	I	Power terminal 1 (5V)
94	VIN1	I	External division into four (DVD/CD) RF input terminal 1
95	VIN2	I	External division into four (DVD/CD) RF input terminal 2
96	VIN3	I	External division into four (DVD/CD) RF input terminal 3
97	VIN4	I	External division into four (DVD/CD) RF input terminal 4
98	VREF4	O	VREF4 voltage output terminal
99	DIFP	O	RF signal (RAM) output terminal P
100	DIFN	O	RF signal (RAM) output terminal N

■ BA5983FM (IC271) : 4CH DRIVER

1. Block Diagram



2. Pin Function

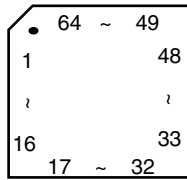
Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	BLAS IN	I	Input for Bias-amplifier	15	VO4(+)	O	Non inverted output of CH4
2	OPIN1(+)	I	Non inverting input for CH1 OP-AMP	16	VO4(-)	O	Inverted output of CH4
3	OPIN1(-)	I	Inverting input for CH1 OP-AMP	17	VO3(+)	O	Non inverted output of CH3
4	OPOUT1	O	Output for CH1 OP-AMP	18	VO3(-)	O	Inverted output of CH3
5	OPIN2(+)	I	Non inverting input for CH2 OP-AMP	19	PowVcc2	-	Vcc for CH3/4 power block
6	OPIN2(-)	I	Inverting input for CH2 OP-AMP	20	STBY2	I	Input for Ch4 stand by control
7	OPOUT2	O	Output for CH2 OP-AMP	21	GND	-	Substrate ground
8	GND	-	Substrate ground	22	OPOUT3	O	Output for CH3 OP-AMP
9	STBY1	I	Input for CH1/2/3 stand by control	23	OPIN3(-)	I	Inverting input for CH3 OP-AMP
10	PowVcc1	-	Vcc for CH1/2 power block	24	OPIN3(+)	I	Non inverting input for CH3 OP-AMP
11	VO2(-)	O	Inverted output of CH2	25	OPOUT4	O	Output for CH4 OP-AMP
12	VO2(+)	O	Non inverted output of CH2	26	OPIN4(-)	I	Inverting input for CH4 OP-AMP
13	VO1(-)	O	Inverted output of CH1	27	OPIN4(+)	I	Non inverting input for CH4 OP-AMP
14	VO1(+)	O	Non inverted output of CH1	28	PreVcc	-	Vcc for pre block

■ JCE8011(IC551):GRAPHIC CONTROLLER

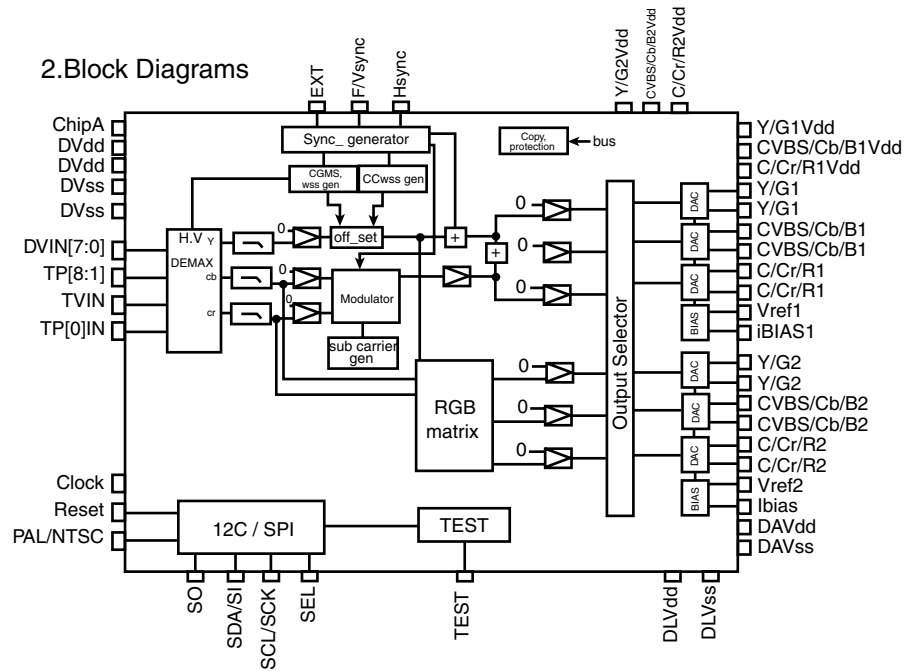
Pin No.	Symbol	I/O	Function
1~8	VD0~7	I	DVD Image signal input (Multi plex data Y,Cr,Cb)
9	VCLKI	I	Dot clock signal input (27MHz)
10	HSYNCI	I	The horizontal synchronous signal input
11	VSYNCI	I	Vertical synchronous signal input
12	VCC	-	Power supply
13	VCLKD	O	Dot clock signal output (27MHz)
14	HSYNCO	O	'H' blanking output
15	VSYNCO	O	'V' blanking output
16~23	DOUT0~7	O	Digital data output
24	TEST	-	Test terminal (Uses as GND usually)
25	RESETB	I	System reset signal
26	GND	-	Connect to GND
27	NTB	I	Mode switching NTSC(low) / PAL(high)
28	DTSF0	I	Taking timing shift of VD input
29	DTSF1	I	Taking timing shift of VD input
30	VIDEG	I	Taking edge specification of VD input (0:up , 1:down)
31	DOSF0	I	Timing shift input of output data
32	DOSF1	I	Timing shift input of output data
33	XVRST	O	Non connect
34	F1	O	Field Identification signal output
35	HBL	O	'H' blanking output
36	VBL	O	'V' blanking output
37	VOEDG	I	Output timing setting of DOUT (0:up , 1:down)
38	VCC	-	Power supply
39~46	FRD7~0	I	Field memory read data input
47	GND	-	Connect to GND
48	FRCK	O	Field memory read clock
49	FWCK	O	Field memory write clock
50	FREB	O	Field memory read enable
51	FWEB	O	Field memory write enable
52	FRRSTB	O	Field memory read address reset
53	FWRSTB	O	Field memory write address reset
54~61	FWD7~0	O	Field memory write data output
62	VCC	-	Power supply
63~70	CHD7~0	I	Character ROM data
71	GND	-	Connect to GND
72	CHOEB	O	Character ROM output enable
73~82	CHA19~10	O	Character ROM address output
83	VCC	-	Power supply
84~93	CHA9~0	O	Character ROM address output
94	GND	-	Connect to GND
95	ACK	O	
96	CS1B	I	Serial data chip select for graphic control
97	CS2B	I	Serial data chip select for encoder control
98	SCK	I	Serial clock input
99	RXD	I	Serial input data
100	TXD	O	Serial output data

MC44724AVFU(IC554):VIDEO ENCODER

1.Terminal Layout



2.Block Diagrams

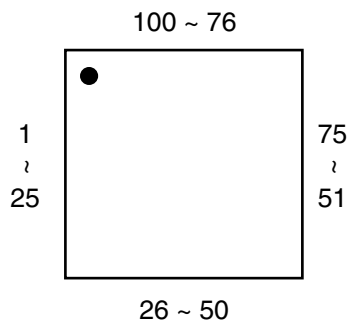


3.Pin function

No.	Symbol	I/O	Function	No.	Symbol	I/O	Function
1	CVBS/Cb/B1	O	Analog composite drive signal (+)	33	SO	-	Non connect
2	CVBS/Cb/B1	O	Analog composite drive signal (-)	34	SDA/SI	I	SPI Mode : Serial data input
3	CVBS/Cb/B1Vdd	-	Power supply for CVBS/Cb/B DAC1	35	SCL/SCK	I	Serial clock input
4	Y/G1	O	Analog brightness signal/G drive signal (+)	36	SEL	I	Power supply for serial data,chip select,digital
5	$\overline{Y/G1}$	O	Analog brightness signal/G drive signal (-)	37	DVdd	--	Power supply for digital circuit
6	Y/G1/Vdd	-	Power supply for Y/G DAC	38	DVss	--	Digital ground
7	C/Cr/R1	O	Analog chroma signal (+)	39	DVIN7	I/O	Y data input / test data I/O
8	$\overline{C/Cr/R1}$	O	Analog chroma signal (-)	40	DVIN6	I/O	Y data input / test data I/O
9	C/Cr/R1Vdd	-	Power supply for C/Cr/RDAC	41	DVIN5	I/O	Y data input / test data I/O
10	DAVss	-	Connect to ground for DAC	42	DVIN4	I/O	Y data input / test data I/O
11	TBIAS1	O	Standard BIAS for DAC1	43	DVIN3	I/O	Y data input / test data I/O
12	Vref1	-	Standard voltage for DAC1	44	DVIN2	I/O	Y data input / test data I/O
13	DAVdd	-	Power supply for DAC	45	DVIN1	I/O	Y data input / test data I/O
14	Vref2	-	Standard voltage for DAC2	46	DVIN0	I/O	Y data input / test data I/O
15	TBIAS2	O	Standard BIAS for DAC2	47	TVIN	I	VIDEO mote on Reset(0:normal, 1:mute)
16	NC	-	Non connect	48	EXT	I/O	Frame output / VBI information input
17	CVBS/Cb/B2	O	Analog composite drive signal (+)	49	F/Vsyac	I/O	Frame / Vertical, synchronous I/O
18	CVBS/Cb/B2	O	Analog composite drive signal (-)	50	Chsyac	I/O	The horizontal, synchronous I/O
19	CVBS/Cb/B2Vdd	-	Power supply for CVBS/Cb/B DAC2	51	DATST	I	Data input
20	Y/G2	O	Analog brightness signal/G drive signal (+)	52	TP-8	I/O	Multiplex data input
21	$\overline{Y/G2}$	O	Analog brightness signal/G drive signal (-)	53	TP7	I/O	Multiplex data input
22	Y/GVdd	-	Power supply for Y/G DAC	54	TP6	I/O	Multiplex data input
23	C/Cr/R2	O	Analog chroma signal (+)	55	TP5	I/O	Multiplex data input
24	$\overline{C/Cr/R2}$	O	Analog chroma signal (-)	56	DVss	-	Ground for digital circuit
25	C/Cr/R2Vdd	-	Power supply for C/Cr/RDAC2	57	DVdd	-	Power supply for digital circuit
26	ChipA	-	Chip address selection	58	TP4	I/O	Data input / Test data I/O
27	TEST	I	Connect to test pin	59	TP3	I/O	Data input / Test data I/O
28	DVdd	-	Digital ground	60	TP2	I/O	Data input / Test data I/O
29	CLOCK	I	Clock signal input (27MHz)	61	TP1	I/O	Data input / Test data I/O
30	DVss	-	Power supply for digital circuit	62	TP0	I/O	Data input / Test data I/O
31	Reset	I	Reset signal input L:ON	63	DLVdd	-	Power supply for D/A converter
32	PAL/NTSC	I	Selection NTSC/PAL NTSC:L PAL:H	64	DLVss	-	Ground for D/A converter

■ MN101C12G (IC701): System micom

1. Terminal layout



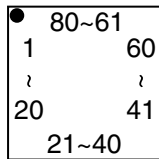
2. Pin function

Pin No.	Symbol	I/O	Function
1	GND	-	GND
2	CS0	I	A set bit0 (It is effective in the U.E version)
3	CS1	I	A set bit1 (It is effective in the U.E version)
4	CS2	I	A set bit2 (It is effective in the U.E version)
5	NTSEL	I	NTSC/PAL switch SW input
6	POWER SW	I	Power key input
7	SHUT1	I	JOG shuttle inout (AD)
8	KEY1-5	I	10 Key input (1~5)
9	KEY6-10	I	10 Key input (6~10, +10)
10	VREF	-	+B (Apply 5V)
11	VDD	-	+B (Apply 5V)
12	OSC2	O	10MHz OSC
13	OSC1	I	10MHz OSC
14	VSS	-	GND
15	-	I	Unused, Connects with GND
16	-	O	Unused
17	MMOD	I	Connects with GND
18	OSDCS3	O	V.ENCODER chip selection
19	RSTE	O	V.ENCOSER reset
20	OSDDO	O	V.ENCODER communication DATA
21	S2UDT	O	Communication between unit microcomputers DATA OUT
22	U2SDT	I	Communication between unit microcomputers DATA IN
23	SCLK	O	Communication between unit microcomputers CLK
24	BUSY	O	Communication between unit microcomputers BUSY
25	CPURST	O	Unit microcomputer reset
26	REQ	I	Communication between unit microcomputers REQ
27	REMO	I	Remote control interruption
28	CS3	I	Set password change judgment bit(H:Change, L:Usual)
29	TEST	I	
30	TEST	I	H:Checkers mode, L:Normal mode
31	TEST	I	H:Running mode, L:Normal mode
32	NC	I	Un used
33	RESET	I	Reset input
34	NC	O	Un used
35	NC	O	Un used
36	VDD	-	Un used
37	OSDCK	O	V.ENCODER communication CK
38	NT	O	

Pin No.	Symbol	I/O	Function
39	FS2	O	48kHz, 96kHz switch
40	CHREQ	I	Changer communication REQUEST
41	CHST	O	Changer communication STROBE
42	CHDATAIO	O	Changer communication DATAI/O
43	NC	-	
44	CHCK	O	Changer communication CLOCK
45	FLDATAO	O	FL driver communication DATAO
46	FLDATAI	I	FL driver communication DATAI
47	FLCK	O	FL driver communication CLOCK
48	FLCS	O	FL driver communication CS
49	FLRST	O	FL reset output
50	EEDO	O	EEPROM communication DATAO
51	EEDI	I	EEPROM communication DATAI
52	EECK	O	EEPROM communication CLOCK
53	EECS	O	EEPROM communication CS
54	VS1	O	S1 control
55	VS3	O	S3 control(STBY:H, P.ON:L)
56	DMUT1	-	Un used
57	DMUT2	-	Un used
58	PDB2	-	Un used
59	PDB2	-	Un used
60	DEMP2	-	Un used
61	DEMP1	-	Un used
62	DENA	-	Un used
63	KARAOKE	O	KARAOKE gain control(At KARAOKE : H)
64	POWERON	O	Power ON output
65	VS2	O	S2 control
66~76	NC	O	Un used
77	AVCI	I	AV COMPULINK input
78	AVCO	O	AV COMPULINK output
79	NC	O	Un used
80	STANBYIND	O	Standby LED output
81~85	NC	O	Un used
86	CS4	O	Un used
87	MA	O	DAC control MA
88	MB	O	DAC control MB
89	M1M3	O	DAC control M1M3
90	MD	O	DAC control MD
91	MC	O	DAC control MC
92	GAIN2	-	Un used
93	GAIN1	-	Un used
94	HPMUT	O	Un used
95	DAVSS	-	Un used
96	LMUTE	O	Un used
97	CMUTE	O	Un used
98	SMUTE	O	Un used
99	MUTE	O	Front mute output
100	DAVDD	-	Apply 5V

■ MN101C15FDD (IC401) : System controller

1. Terminal layout



2. Pin function

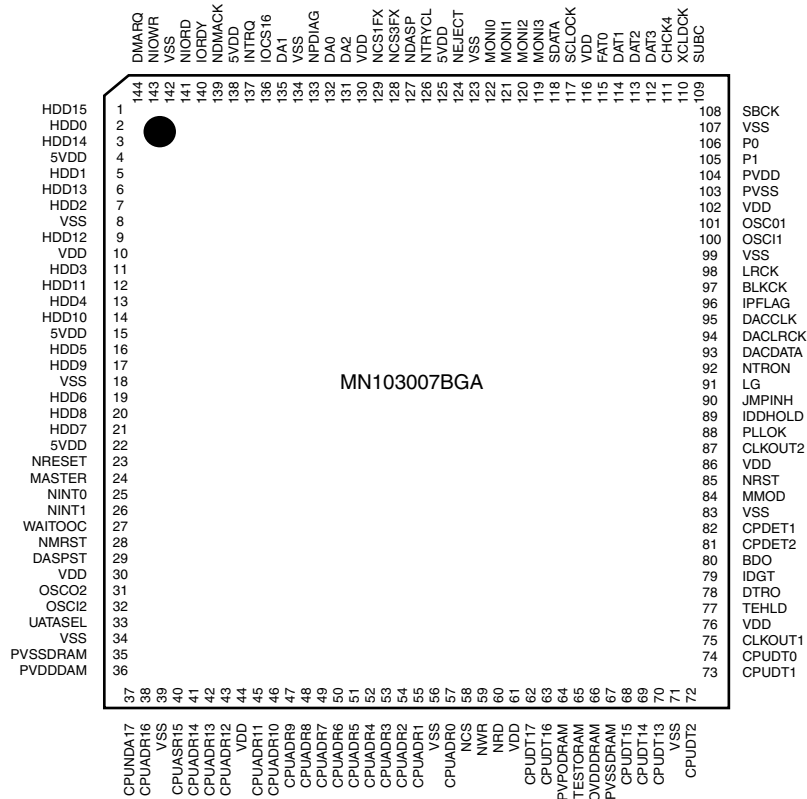
Pin No	Symbol	Function	Pin No	Symbol	Function
1		Ground connection	41	S-MUTE	System mute
2	DVD-S/C	DVD S/C selection terminal	42		Terminal (unused)
3	VCR-S/C	VCR S/C selection terminal	43	T-MUTE	Tuner mute
4		Ground connection	44		Terminal (unused)
5		Ground connection	45		Terminal (unused)
6		Ground connection	46		Terminal (unused)
7		Ground connection	47	RDS-DATA	RDS control signal terminal
8		Ground connection	48		Terminal (unused)
9	PROTECTOR IN	Protector input	49	INHIBIT IN	Inhibit signal input
10	VREF+	Ground connection	50	DSP-READY	DSP control signal
11	VDD	Power supply terminal	51	DSP-RESET	DSP reset signal
12	OSC 2	Quartz oscillation terminal (8 MHz)	52	M/CS	Control signal from IC400
13	OSC 1	Quartz oscillation terminal (8 MHz)	53	M-RESET	Reset signal from IC400
14	VSS	Ground connection	54	M-STATUS	Status signal from IC400
15	X1	Ground connection	55	M-COMMAND	Command signal from IC400
16	X0	Terminal (unused)	56	M-CLK	Clock signal from IC400
17	MMOD	Ground connection	57		Terminal (unused)
18		Terminal (unused)	58		Terminal (unused)
19		Ground connection	59		Terminal (unused)
20		Ground connection	60		Terminal (unused)
21	DSP-COMMAND	DSP control signal terminal	61	SW-DATA	Data signal for source selector
22	DSP-STATUS	DSP control signal terminal	62	SW-CLK	Clock signal for source selector
23	DSP-CLK	DSP control signal terminal	63	VOL-STB	Strop signal for controlling volume
24		Ground connection	64	VOL-DATA	Data signal for controlling volume
25	RESET-IN	Reset signal input terminal	65	VOL-CLK	Clock signal for controlling volume
26	TUNER-CE	Tuner chip enable	66	SW-STB	Strop signal for source selector
27	TUNER-CLK	Tuner clock signal input	67		Terminal (unused)
28		Ground connection	68	SWF MUTE	Sub woofer mute
29	TUNER-DATA	Tuner control terminal	69	SURR	Terminal (unused)
30	RDS SCL	Clock signal (RDS)	70	FR-RELAY	Front speaker relay control
31	TUNER-IN	Tuner signal input terminal	71	CNTR-RELAY	Center speaker relay control
32	STEREO-IN	Stereo signal input terminal	72	SUR-RELAY	Rear speaker relay control
33	RDS-ST	Terminal (unused)	73		Terminal (unused)
34	M-BUSY	Busy signal from IC400 input	74		Ground connection
35	RDSCLOCKIN	Ground connection	75		Ground connection
36		Terminal (unused)	76		Ground connection
37		Terminal (unused)	77		Ground connection
38		Terminal (unused)	78	LED	Terminal (unused)
39	VIDEO1	VIDEO 1 signal	79	D.AUT LED	Indicate control (DIGITAL AUTO)
40	VIDEO2	VIDEO 2 signal	80	SURR LED	Indicate control (SURROUND)

■ MN102L25GCY(IC401):UNIT CPU

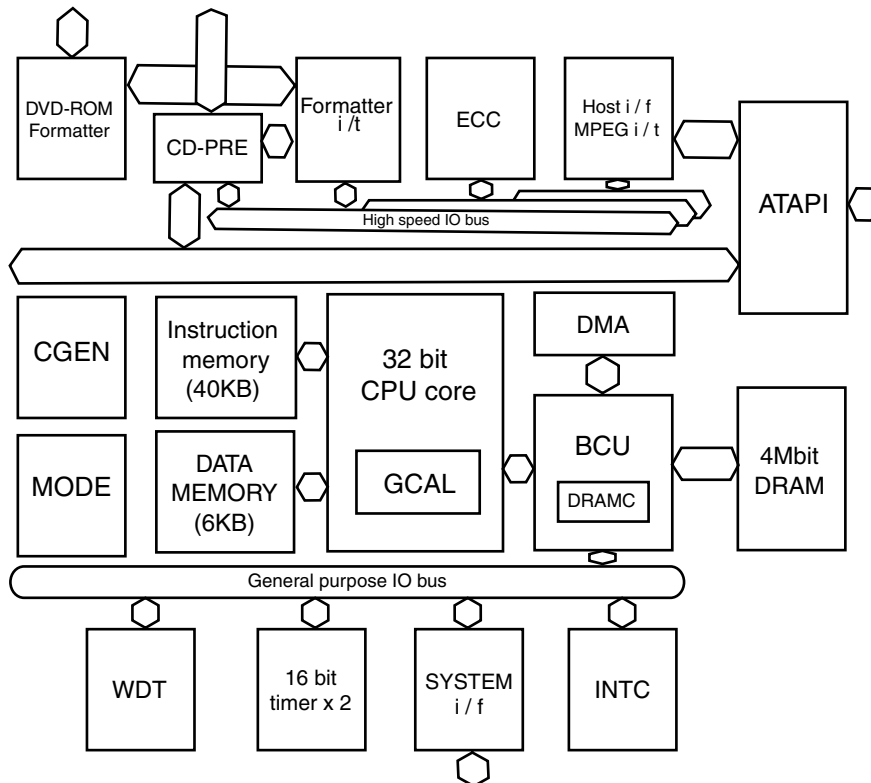
Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	WAIT	I	Micon wait signal input	51	FGIN	I	Photo input
2	RE	O	Read enable	52	-		Non connect
3	MUTE	O	Driver mute	53	ADSCEN	O	Serial enable signal for ADSC
4	WEM	O	Write enable	54	VDD	-	Non connect
5	CS0	O	Non connect	55	FEPEN	O	Serial enable signal for FEP
6	CS1	O	Chip select for ODC	56	SLEEP	O	Standby signal for FEP
7	CS2	O	Chip select for ZIVA	57	BUSY	I	Communication busy
8	CS3	O	Chip select for outer ROM	58	REQ	O	Communication Request
9	FGCONT	O	Photo control	59	CIRCEN	O	CIRC command select
10	/SPKICK	O	Spin kick	60	HSSEEK	O	Seek select
11	LSIRST	O	LSI reset	61	VSS	-	Power supply
12	WORD	O	Bus selection input	62	EPCS	O	EEPROM chip select
13	A0	O	Address bus 0 for CPU	63	EPSK	O	EEPROM clock
14	A1	O	Address bus 1 for CPU	64	DPDI	I	EEPROM data input
15	A2	O	Address bus 2 for CPU	65	EPDO	O	EEPROM data output
16	A3	O	Address bus 3 for CPU	66	VDD	-	Power supply
17	VDD	-	Power supply	67	SCLK0	I	Communication clock
18	SYSCLK	O	System clock signal output	68	S2UDT	I	Communication input data
19	VSS	-	Power supply	69	U2SDT	O	Communication output data
20	XI	-	Non connect	70	CPSCK	O	Clock for ADSC serial
21	XO	-	Non connect	71	SDIN	I	ADSC serial data input
22	VDD	-	Power supply	72	SDOUT	O	ADSC serial data output
23	OSCI	I	Clock signal input(13.5MHz)	73	-	-	Non connect
24	OSCO	-	Non connect	74	-	-	Non connect
25	MODE	I	CPU Mode selection input	75	NMI	-	Non connect
26	A4	O	Address bus 4 for CPU	76	ADSCIRQ	I	Interrupt input of ADSC
27	A5	O	Address bus 5 for CPU	77	ODCIRQ	I	Interrupt input of ODC
28	A6	O	Address bus 6 for CPU	78	DECIRQ	I	Interrupt input of ZIVA
29	A7	O	Address bus 7 for CPU	79	WAKEUP	O	Non connect
30	A8	O	Address bus 8 for CPU	80	ODCIRQ2	I	Non connect
31	A9	O	Address bus 9 for CPU	81	ADSEP	I	Address data selection input
32	A10	O	Address bus 10 for CPU	82	RST	I	Reset input
33	A11	O	Address bus 11 for CPU	83	VDD	-	Power supply
34	VDD	-	Power supply	84	TEST1	I	Test signal 1 input
35	A12	O	Address bus 12 for CPU	85	TEST2	I	Test signal 2 input
36	A13	O	Address bus 13 for CPU	86	TEST3	I	Test signal 3 input
37	A14	O	Address bus 14 for CPU	87	TEST4	I	Test signal 4 input
38	A15	O	Address bus 15 for CPU	88	TEST5	I	Test signal 5 input
39	A16	O	Address bus 16 for CPU	89	TEST6	I	Test signal 6 input
40	A17	O	Address bus 17 for CPU	90	TEST7	I	Test signal 7 input
41	A18	O	Address bus 18 for CPU	91	TEST8	I	Test signal 8 input
42	A19	O	Address bus 19 for CPU	92	VSS	-	Power supply
43	VSS	-	Power supply	93	D0	I/O	Data bus 0 of CPU
44	A20	O	Address bus 20 for CPU	94	D1	I/O	Data bus 1 of CPU
45	TXSEL	O	TX Select	95	D2	I/O	Data bus 2 of CPU
46	TMPSN	O	Non connect	96	D3	I/O	Data bus 3 of CPU
47	-		Non connect	97	D4	I/O	Data bus 4 of CPU
48	ADPD	O	AD Power down	98	D5	I/O	Data bus 5 of CPU
49	-		Non connect	99	D6	I/O	Data bus 6 of CPU
50	TRVSW	I	Detection switch of traverse inside	100	D7	I/O	Data bus 7 of CPU

MN103007BGA (IC301) : Optical disc controller

1. Terminal layout



2. Block diagram



3.Function

MN103007BGA(1/2)

Pin NO.	Symbol	I/O	Function	Pin NO.	Symbol	I/O	Function
1	HDD15	I/O	ATAPI data	48	CPUADR8	I	System control address
2	HDD0	I/O	ATAPI data	49	CPUADR7	I	System control address
3	HDD14	I/O	ATAPI data	50	CPUADR6	I	System control address
4	5VDD			51	CPUADR5	I	System control address
5	HDD1	I/O	ATAPI data	52	CPUADR4	I	System control address
6	HDD13	I/O	ATAPI data	53	CPUADR3	I	System control address
7	HDD2	I/O	ATAPI data	54	CPUADR2	I	System control address
8	VSS			55	CPUADR1	I	System control address
9	HDD12	I/O	ATAPI data	56	VSS		GND
10	VDD			57	CPUADR0	I	System control address
11	HDD3	I/O	ATAPI data	58	NCS	I	System control chip selection
12	HDD11	I/O	ATAPI data	59	NWR	I	System control wright
13	HDD4	I/O	ATAPI data	60	NRD	I	System control lead
14	HDD10	I/O	ATAPI data	61	VDD		Apply 3V
15	5VDD			62	CPUDT7		System control data
16	HDD5	I/O	ATAPI data	63	CPUDT6		System control data
17	HDD9	I/O	ATAPI data	64	PVPPDRAM	O	C=10000PF is connected between VSS
18	VSS						
19	HDD6	I/O	ATAPI data	65	PTESTDRAM	I	VSS connected
20	HDD8	I/O	ATAPI data	66	OVDDDRAM		
21	HDD7	I/O	ATAPI data	67	PVSSDRAM		
22	5VDD			68	CPUDT5		System control data
23	NRESET	I	ATAPI reset	69	CPUDT4		System control data
24	MASTER	I/O	ATAPI master / slave selection	70	CPUDT3		System control data
25	NINT0	O	System control interruption 0	71	VSS		GND
26	NINT1	O	System control interruption 1	72	CPUDT2		System control data
27	WAITODC	O	System control weight control	73	CPUDT1	I/O	System control data
28	NMRST	O	System control reset	74	CPUDT0	I/O	System control data
29	DASPST	I	DASP signal initializing	75	CLKOUT1	O	16.9/11.2/8.45MHz clock
30	VDD			76	VDD	-	Apply 3V
31	OSCO2	I,O	VSS connection, OPEN	77	TEHLD	O	Mirror gate
32	OSCI2	I,O	VSS connection, OPEN	78	DTRO	O	Data part frequency control switch
33	UATASEL	I	VSS connection				
34	VSS			79	IDGT	O	Part CAPA switch
35	PVSSDRAM			80	BDO	I	RF dropout / BCA data of making to binary
36	PVDODRAM						
37	CPUADR17	I	System control address	81	CPDET2	I	Outer side CAPA detection
38	CPUADR18	I	System control address	82	CPDET1	I	Side of surroundings on inside
39	VSS			83	VSS		GND
40	CPUADR15	I	System control address	84	MMOD	I	VSS connected
41	CPUADR14	I	System control address	85	NRST	I	System reset
42	CPUADR13	I	System control address	86	VDD	-	Apply 3V
43	CPUADR12	I	System control address	87	CLKOUT2	O	16.9MHz clock
44	VDD		System control address	88	PLLOK	O	Frame mark detection
45	CPUADR11	I	System control address	89	IDOHOLD	O	ID gate for tracking holding
46	CPUADR10	I	System control address	90	JMPINH	O	Jump prohibition
47	CPUADR9	I	System control address				

Pin NO.	Symbol	I/O	Function	Pin NO.	Symbol	I/O	Function
91	LG	O	Land / group switch	133	NPDIAG	I/O	ATAPI slave master diagnosis input
92	NTRON	I	Tracking ON	134	VSS		
93	DACDATA	O	Cereal output	135	DA1	I/O	ATAPI host address
94	DACLCK	O	L and R identification output	136	IOCS16	O	ATAPI output of selection of width of host data bus
95	DACCLK	I	Clock for cereal output				
96	IPFLAG	I	Interpolation flag input	137	INTRQ	O	ATAPI host interruption output
97	BLKCK	I	Sub-code,Block clock input	138	5VDD		
98	LRCK	I	L and R identification signal output	139	NDMACK	I	ATAPI host DMA response
99	VSS			140	IORDY	O	ATAPI host ready output
100	OSCI1	I,O	16.9MHz oscillation	141	NIORD	I	ATAPI host read
101	OSCO1	I,O	16.9MHz oscillation	142	VSS		
102	VDD			143	NIOWR	I/O	ATAPI host writes
103	PVSS			144	DMARQ	O	ATAPI host DMA demand
104	PVDD						
105	P1	I/O	Terminal MASTER polarity switch input				
106	P0	I/O	CIRC-RAM OVER/UNDER Interruption signal input				
107	VSS						
108	SBCK	O	Sub-code, Clock output for serial input				
109	SUBC	I	Sub-code, Cereal input				
110	XCLDCK	I	Sub-code, Frame clock input				
111	CHCK4	I	Read clock to DAT3~0(Output of dividing frequency four from ADSC)				
112	DAT3	I	Read data from DISC (PARalle output from ADSC)				
113	DAT2	I					
114	DAT1	I					
115	DAT0	I					
116	VDD						
117	SCLOCK	I/O	Debugging cereal clock (270 Ω pull up)				
118	SDATA	I/O	Debugging cereal data (270 Ω pull up)				
119~122	MONI3~0	O	Internal goods title monitor				
123	VSS						
124	NEJECT	I	Eject detection				
125	5VDD						
126	NTRYCL	I	Tray close detection				
127	NDASP	I/O	ATAPI Drive active/ Slave connection I/O				
128	NCS3FX	I	ATAPI host chip selection				
129	NCS1FX	I	ATAPI host chip selection				
130	VDD						
131	DA2	I/O	ATAPI host address				
132	DA0	I/O	ATAPI host address				

Pin NO.	Symbol	I/O	Function
91	LG	O	Land / group switch
92	NTRON	I	Tracking ON
93	DACDATA	O	Cereal output
94	DACLCK	O	L and R identification output
95	DACCLK	I	Clock for cereal output
96	IPFLAG	I	Interpolation flag input
97	BLKCK	I	Sub-code,Block clock input
98	LRCK	I	L and R identification signal output
99	VSS		
100	OSC11	I,O	16.9MHz oscillation
101	OSCO1	I,O	16.9MHz oscillation
102	VDD		
103	PVSS		
104	PVDD		
105	P1	I/O	Terminal MASTER polarity switch input
106	P0	I/O	CIRC-RAM OVER/UNDER Interruption signal input
107	VSS		
108	SBCK	O	Sub-code, Clock output for serial input
109	SUBC	I	Sub-code, Cereal input
110	XCLDCK	I	Sub-code, Frame clock input
111	CHCK4	I	Read clock to DAT3~0 (Output of dividing frequency four from ADSC)
112	DAT3	I	Read data from DISC (PARalle output from ADSC)
113	DAT2	I	
114	DAT1	I	
115	DAT0	I	
116	VDD		
117	SCLOCK	I/O	Debugging cereal clock (270Ω pull up)
118	SDATA	I/O	Debugging cereal data (270Ω pull up)
119	MONI3	O	Internal goods title monitor
120	MONI2	O	
121	MONI1	O	
122	MONI0	O	
123	VSS		
124	NEJECT	I	Eject detection
125	5VDD		
126	NTRYCL	I	Tray close detection
127	NDASP	I/O	ATAPI Drive active/ Sulave connection I/O
128	NCS3FX	I	ATAPI host chip selection
129	NCS1FX	I	ATAPI host chip selection
130	VDD		
131	DA2	I/O	ATAPI host address
132	DA0	I/O	ATAPI host address

Pin NO.	Symbol	I/O	Function
133	NPDIAG	I/O	ATAPI slave master diagnosis input
134	VSS		
135	DA1	I/O	ATAPI host address
136	IOCS16	O	ATAPI output of selection of width of host data bus
137	INTRQ	O	ATAPI host interruption output
138	5VDD		
139	NDMACK	I	ATAPI host DMA response
140	IORDY	O	ATAPI host ready output
141	NIORD	I	ATAPI host read
142	VSS		
143	NIOWR	I/O	ATAPI host writes
144	DMARQ	O	ATAPI host DMA demand

■ MN173222DF (IC400): Operation Switches and Fluorescent Display Controller

1. Key matrix

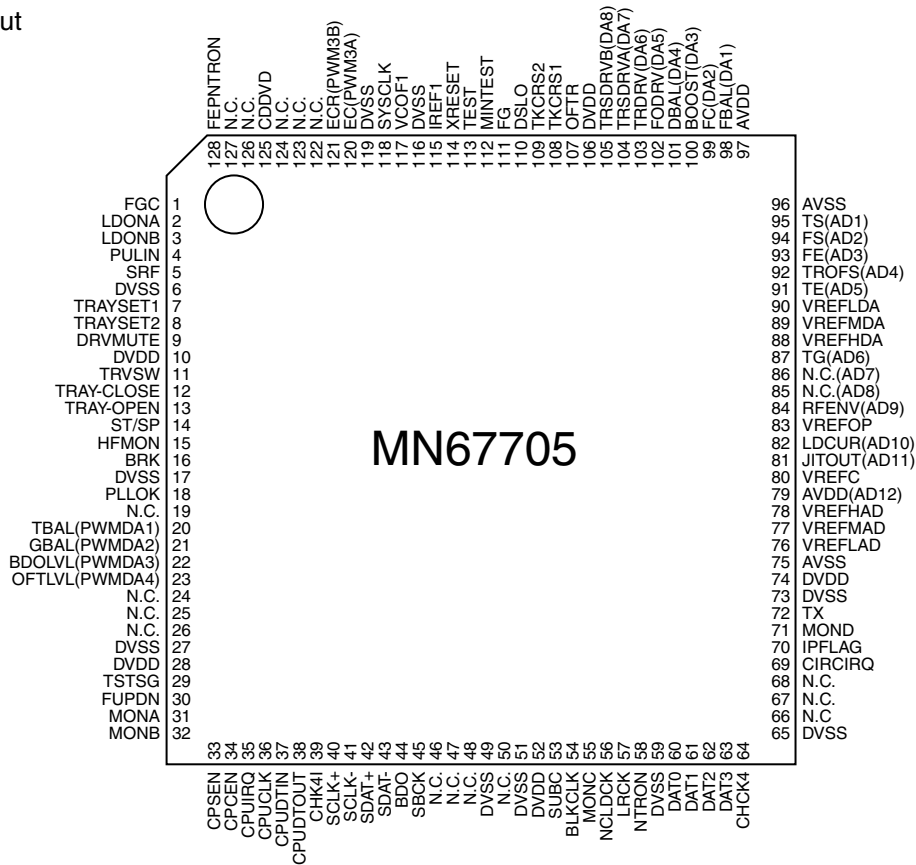
	KEY OUT 0	KEY OUT1	KEY OUT 2	KEY OUT 3	KEY OUT 4
KEY IN 0	POWER	DSP MODE	DVD	←	CD
KEY IN 1	ADJUST	SURROUND	TV SOUND/DBS	→	PHONE
KEY IN 2	SETTING	ANALOG/DIGITAL	VCR	↑	TAPE/MD
KEY IN 3	MEMORY	—————	ONE TOUCH OP. /INPUT ATT.	↓	FM/AM

2. Pin function

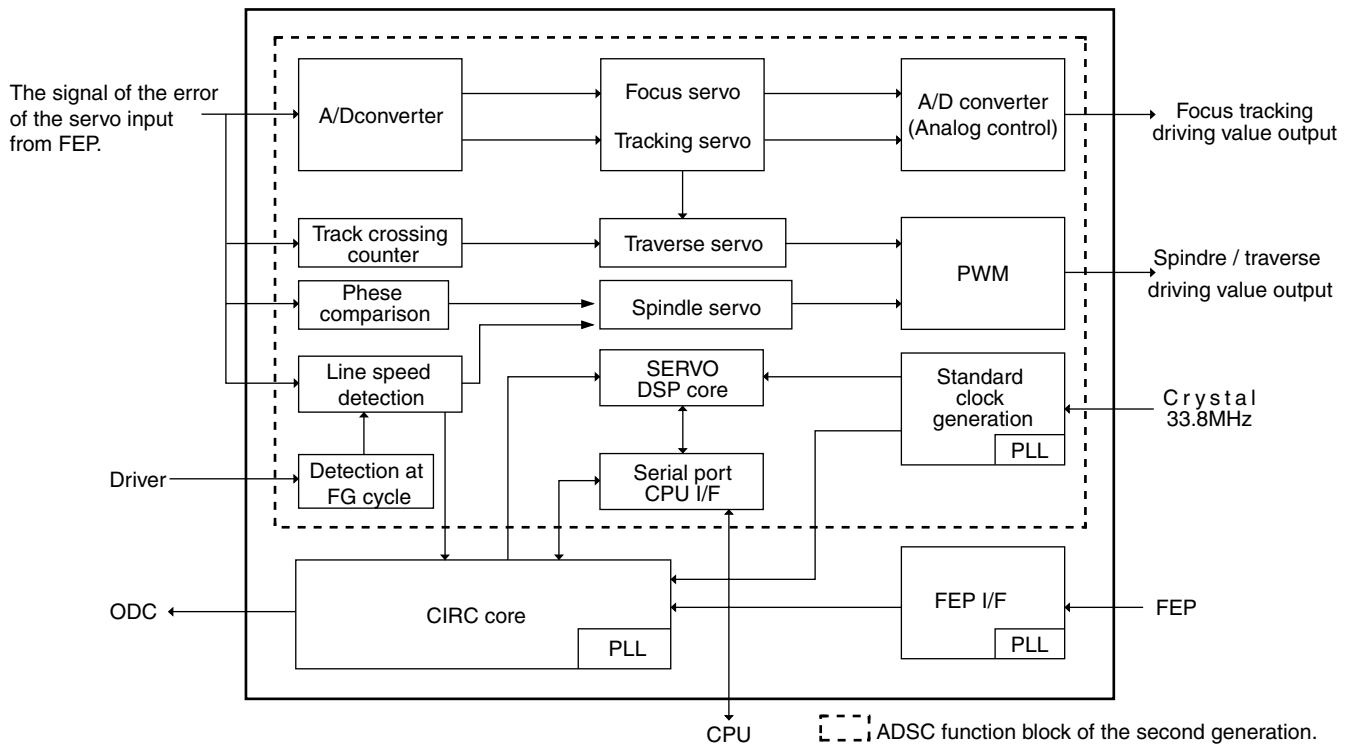
Pin No.	Symbol	I/O	Functions
1-22	S22-S1	O	Segment control signal output
23	VPP	-	Power supply terminal
24-29	KO0-5/G14-9	O	Key matrix output/grid control signal output
30,31	G8,G7	O	Grid control signal output
32,33	SW0,1/G6,5	O	Grid control signal output
34-36	G4-G2	O	Grid control signal output
37-39	G16,15,1	O	Grid control signal output
40,41		-	Ground connection
42	JOG1,2	I	JOG volume control input
44	MBUSY	I	Busy signal from IC401
45	MCLK	I	Clock signal from IC401
46	COMMAND	I	Command data input from IC401
47	STATUS	O	Status signal output to IC401
48	M/CS	I	Chip select signal input from IC401
49	RM	I	Remote control signal input
50	VCRI	I	AV COMPULINK input (VCR)
51	DCSI	I	COMPULINK signal input
52	DCSO	O	COMPULINK signal output
53	VCRO	O	AV COMPULINK output (VCR)
54	TVO	O	AV COMPULINK output (TV)
55	TVC	O	AV COMPULINK control output
56,57		-	Ground connection
58	POWER	-	Power supply terminal
59	STANDBY	O	Stand-by indicator control
60-63	KI3-KI0	I	Key matrix input
64-67	S36-S33	O	Segment control signal output
68	RST	I	Reset signal input
69	X1		Ground connection
70	X2		Terminal (unused)
71	VSS	-	Ground connection
72,73	OSC2,1	-	Quartz oscillation terminal (6 MHz)
74	VDD	-	Power supply terminal
75-84	S32-S23	O	Segment control signal output

MN67705EA (IC201) : Digital servo controller

1. Terminal layout



2. Block diagram



3.Pin function

MN67705EA (1/3)

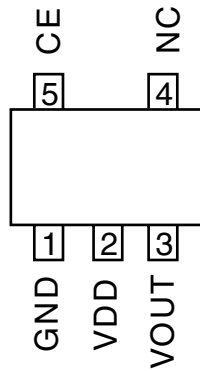
PinNo.	Symbol	I/O	Function
1	FGC	0	H fixation
2	LDONA	O	Laser drive controlA (ON / OFF)
3	LDONB	O	Laser drive controlB (ON / OFF)
4	PULIN	O	DSL and PLL high boost signal (FEP)
5	SRF	O	Head amplifier gain H/L selection
6	DVSS	—	Ground for digital circuit
7	TRAYSET1	O	Tray drive ON/OFF and direction control
8	TRAYSET2	O	Tray drive ON/OFF and direction control
9	DRVMUTE	O	Drive IC mute control
10	DVDD	—	Power supply for digital circuit
11	TRVSW	I	Surroundings position detection in traverse
12	TRAY-CLOSE	I	Tray close detection SW
13	TRAY-OPEN	I	Tray opening detection SW
14	ST/SP	O	Spindle motor drive switch (START /STOP)
15	HFMON	O	High cycle module control
16	BRK	O	Spindle motor IC short brake control
17	DVSS	—	Ground for digital circuit
18	PLLOK	I	SYNC detection (DVD : 18T / CD : 22T)
19	N.C.	O	
20	TBAL(PWMDA1)	O	Tracking balance (FEP)
21	GBAL(PWMDA2)	O	Tangential balance (FEP)
22	BDOLVL(PWMDA3)	O	BDO slice level (FEP)
23	OFTLVL(PWMDA4)	O	Off-track error slice level (FEP)
24	N.C.	O	
25	N.C.	O	
26	N.C.	O	
27	DVSS	—	Ground for digital circuit
28	DVDD	—	Power supply for digital circuit
29	TSTSG	O	Self calibration signal (FEP)
30	FUPDN	O	Signal of frequency UP/DOWN of PLL (FEP)
31	MONA	O	Monitor terminal A
32	MONB	O	Monitor terminal B
33	CPSEN	I	Servo DSP cereal I/F chip selection (SYSCOM)
34	CPCEN	I	CIRC cereal I/F chip selection (SYSCOM)
35	CPUIRQ	O	Interrupt request to silicon (SYSCOM)
36	CPUCLK	I	Silicon cereal I/F clock (SYSCOM)
37	CPUDTIN	I	Silicon cereal I/F data input (SYSCOM)
38	CPUDTOUT	O	Silicon cereal I/F data output (SYSCOM)
39	CHK4I	I	Connects with unused DVSS
40	SCLK+	I	Lead channel clock differential motion signal (positive)
41	SCLK-	I	Lead channel clock differential motion signal (negative)
42	SDAT+	I	Lead channel data differential motion signal (positive)
43	SDAT-	I	Lead channel data differential motion signal (negative)
44	BDO	I	BDO + BCA (FEP)
45	SBCK	I	CD sub-code data shift clock (ODC)
46	IREF2	—	Connects with unused DVSS

Pin No.	Symbol	I/O	Function
47	IREF3	—	Connects with unused DVSS
48	VCOF2	—	Connects with unused DVSS
49	DVSS	—	Ground for digital circuit
50	VCOE3	—	Connects with unused DVSS
51	DVSS	—	Ground for digital circuit
52	DVDD	—	Power supply for digital circuit
53	SUBC	O	CD sub-code (ODC)
54	BLKCLK	O	CD sub-code synchronous signal (ODC)/Jump output of one at DVD
55	MONC	O	Monitor terminal C
56	NCLDCK	O	Sub-code data frame clock (ODC)
57	LRCK	O	LR channel data strobe circCIRC(ODC)
58	NTRON	O	L: Tracking ON (ODC)
59	DVSS	—	Ground for digital circuit
60	DAT0	O	CIRC / Binary making DVD data output
61	DAT1	O	CIRC / Binary making DVD data output
62	DAT2	O	CIRC / Binary making DVD data output
63	DAT3	O	CIRC / Binary making DVD data output
64	CHCK4	O	Synchronous clock of DAT0~3
65	DVSS	—	Ground for digital circuit
66	DACCLK	O	
67	DACLCK	I	Connects with unused DVSS
68	DACDATA	I	Connects with unused DVSS
69	CIRCIRQ	O	RAM with built-in CIRC exceeds / Underflow interrupt
70	IPFLAG	O	CIRC error flag
71	MOND	O	Monitor terminal D
72	TX	O	Digital audio interface
73	DVSS	—	Ground for digital circuit
74	DVDD	—	Power supply for digital circuit
75	AVSS	—	Ground for analog circuit
76	VREFLAD	—	AD subordinate position standard voltage ($0.6 \pm 0.1\text{v}$)
77	VREFMAD	—	It is a place standard voltage in AD ($1.4 \pm 0.1\text{V}$)
78	VREFHAD	—	High-ranking AD standard voltage ($2.2 \pm 0.1\text{V}$)
79	AVDD	—	Power supply for analog circuit
80	VREFC(AD12)	I	
81	JIOUT(AD11)	I	Jitter signal(FEP)
82	LDCUR(AD10)	I	Laser drive current signal
83	VREFOP	—	Operation amplifier standard voltage(VREFC)
84	RFENV(AD9)	I	RFENV(FEP)
85	N.C.(AD8)	I	Connects with VREFC
86	N.C.(AD7)	I	Connects with VREFC
87	TG(AD6)	I	Tangential Phase difference (FEP)
88	VREFHDA	—	High-ranking AD standard voltage ($2.2 \pm 0.1\text{V}$)
89	VREFMDA	—	It is a place standard voltage in AD ($1.4 \pm 0.1\text{V}$)
90	VREFLDA	—	AD subordinate position standard voltage ($0.6 \pm 0.1\text{v}$)
91	TE(AD5)	I	Tracking error (FEP)
92	TROFS(AD4)	I	Tracking drive IC input offset
93	FE(AD3)	I	Focus error (FEP)

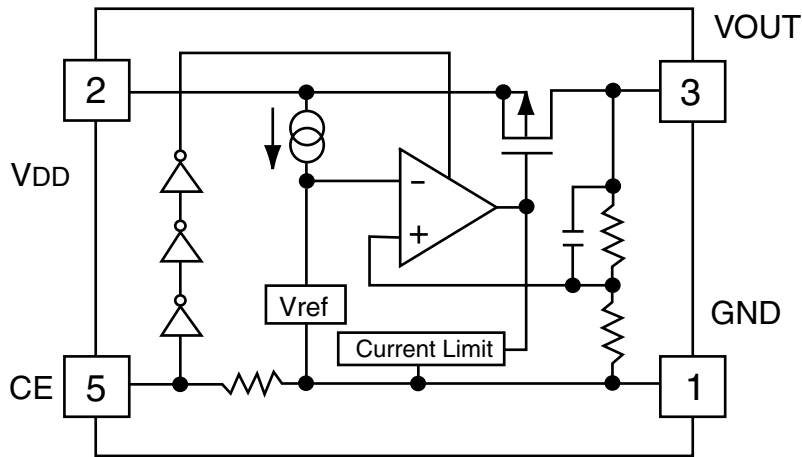
PinNo.	Symbol	I/O	Function
94	FS(AD2)	I	FS (FEP)
95	TS(AD1)	I	TS (FEP)
96	AVSS	—	Ground for analog circuit
97	AVDD	—	Power supply for analog circuit
98	FBAL(DA1)	O	Focus balance(FEP)
99	FC(DA2)	O	Cutting off frequency (FEP)
100	BOOST(DA3)	O	Amount of boost (FEP)
101	TBAL(DA4)	O	DSL offset balance (FEP)
102	FODRV(DA5)	O	Focus drive
103	TRDRV(DA6)	O	Tracking drive
104	TRSDRVA(DA7)	O	Traverse drive A aspect
105	TRSDRVB(DA8)	O	Traverse drive B aspect
106	DVDD	—	Power supply for digital circuit
107	OFTR	I	Off-track error signal (FEP)
108	TKCRS1	I	Track crossing signal 1 (FEP)
109	TKCRS2	I	Track crossing signal 2 (FEP)
110	DSLO	I	Binary making data slice signal (FEP)
111	FG	I	FG signal input (spindle motor driver)
112	MINTEST	—	Connects with DVSS
113	TEST	—	Connects with DVSS
114	XRESET	I	Reset L : Reset
115	IREF1	—	VCO reference current 1(for SYSCLK)
116	DVSS	—	Ground for digital circuit)
117	VCOF1	—	VCO control voltage 1 (for SYSCLK)
118	SYSCLK	I	33.8MHz system clock input
119	DVSS	—	Ground for digital circuit
120	EC(PWM3A)	O	Spindle motor drive
121	ECR(PWM3B)	O	
122	N.C.(PWM3A)	O	
123	N.C.(PWM2B)	O	
124	N.C.(PWM1A)	O	
125	CDDVD	O	CD/DVD control signal (FEP) CD : H DVD : L
126	N.C.(PWM0A)	O	
127	N.C.(PWM0B)	O	
128	FEPNTRON	O	Tracking ON (FEP)

■ RN5RZ20BA-X(IC102) : High cycle module

1. Terminal layout



2. Block diagram

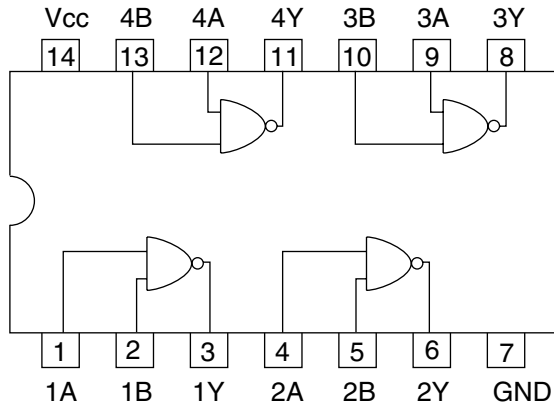


3. Pin function

Pin No.	Pin name	Function
1	GND	Ground terminal
2	VDD	Input terminal
3	VOUT	Output terminal
4	NC	No connection
5	CE	Chip enable terminal

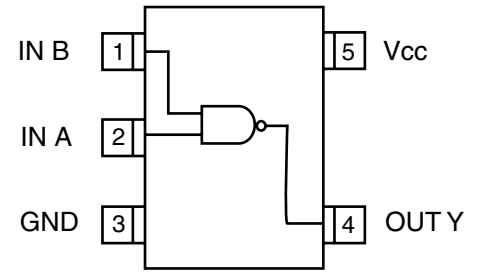
■ **TC74VHC00FT-X(IC503) : Wright timing control**

1. Terminal layout / Block diagram



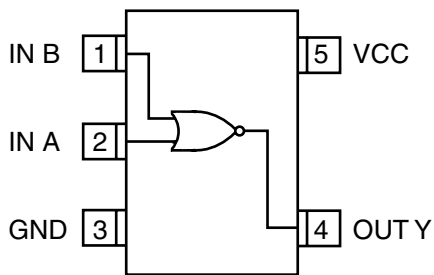
■ **TC7SH04FU (IC107) :**

1. Terminal layout



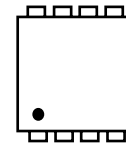
■ **TC7SH32FU-X(IC312) : Timing control**

1. Terminal layout

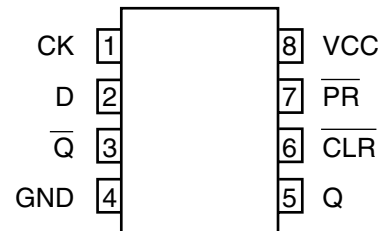


■ **TC7WH74FU-X(IC374) : Clock buffer**

1. Terminal layout

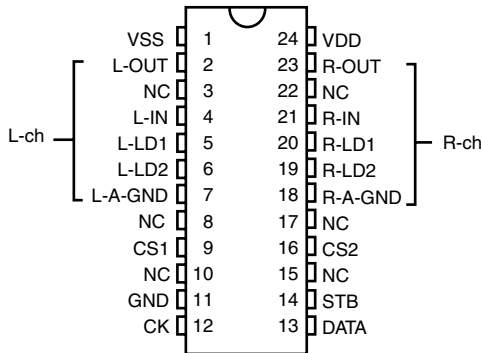


2. Block diagram

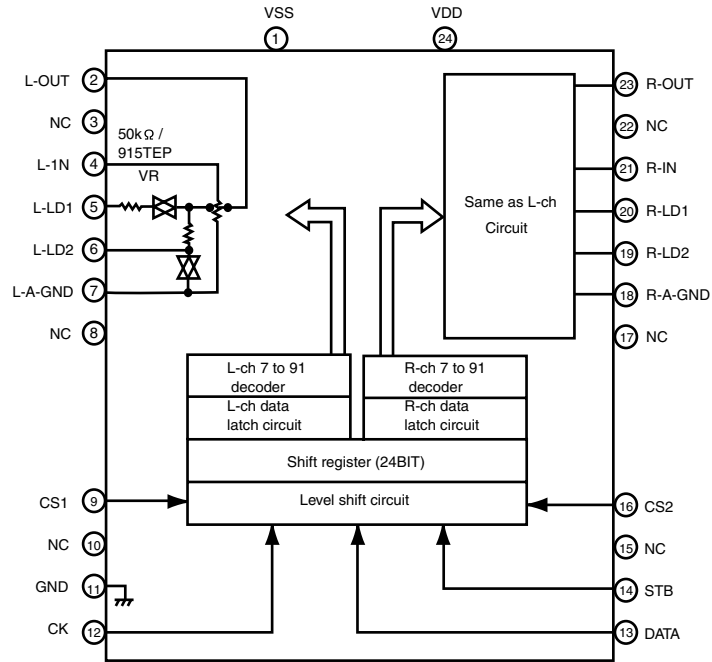


■ TC9459F (IC331,IC332,IC333) : Electronic volume control

1. Terminal layout



2. Block diagram

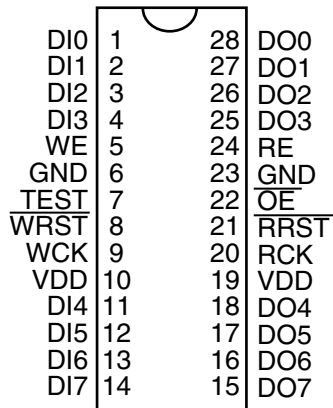


3. Pin function

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	VSS	Negative power supply pin	13	DATA	Data input pin
2	L-OUT	Volume output pin	14	STB	Strobe input pin
3	NC	No connection	15	NC	No connection
4	NC	No connection	16	CS2	Chip select input pin
5	L-LD1	Loudness tap output pin	17	NC	No connection
6	L-LD2	Loudness tap output pin	18	R-A-GND	Analog GND pin
7	L-A-GND	Analog GND pin	19	R-LD2	Loudness tap output pin
8	NC	No connection	20	R-LD1	Loudness tap output pin
9	CS1	Chip select input pin	21	R-IN	Volume input pin
10	NC	No connection	22	NC	No connection
11	NC	No connection	23	R-OUT	Volume output pin
12	CK	Clock input pin	24	VDD	Positive power supply pin

■ UPD42280GU-30-X(IC552):2M RAM

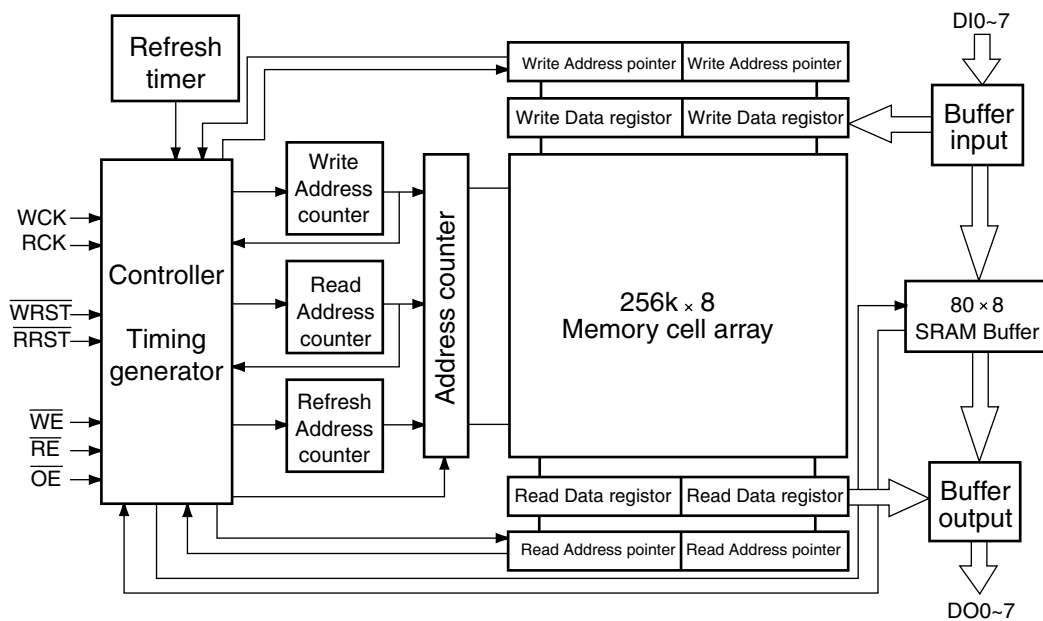
1. Terminal Layout



2. Pin Function

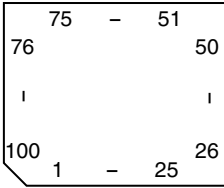
Pin No.	Symbol	I/O	Pin Function
1~4	DI0~3	I	Data input
5	WE	I	Write enable signal input
6	GND	-	Connect to GND
7	TEST	-	Connect to GND
8	WRST	I	Write reset signal input
9	WCK	I	Write clock signal input
10	VDD	-	Power supply +5V
11~14	DI4~7	I	Data input
15~18	DO7~4	O	Data output
19	VDD	-	Power supply +5V
20	RCK	I	Read clock signal input
21	RRST	I	Read reset signal input
22	OE	-	Connect to GND
23	GND	-	Connect to GND
24	RE	I	Read enable signal input
25~28	DO3~0	O	Data output

3. Block Diagrams



■ UPD784215AGC102(IC671): DSP Controller

1. Terminal layout

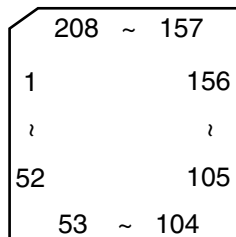


2. Pin function

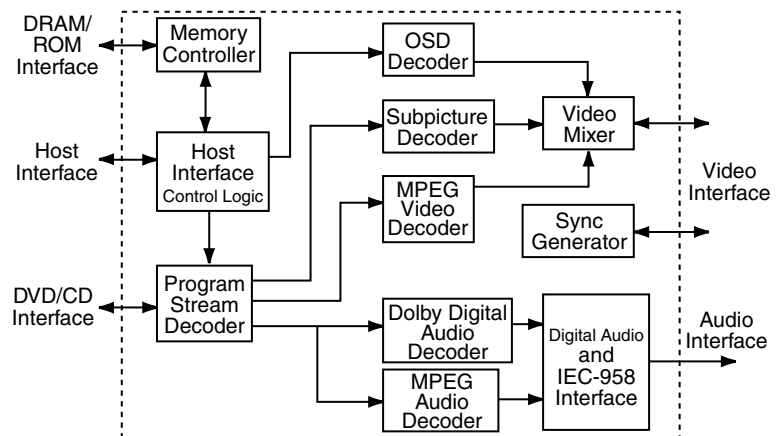
Pin No.	Symbol	I/O	Functions
1-8		-	Terminal (unused)
9	VDD	-	Power supply terminal
10	X2	O	Quartz oscillation terminal 6.14 MHz (Main clock)
11	X1	I	Quartz oscillation terminal 6.14 MHz (Main clock)
12	VSS	-	Ground connection
13	XT2	-	Terminal (unused)
14	XT1	-	Terminal (unused)
15	RESET	I	Reset signal input
16	AUTODATA	I	DSP general-purpose port output interruption
17	LOCK	I	DSP general-purpose port output interruption
18	DIGITAL0	I	DSP general-purpose port output interruption
19	FORMAT	I	DSP general-purpose port output interruption
20	CHANNEL	I	DSP general-purpose port output interruption
21	ERR	I	DSP general-purpose port output interruption
22	RSTDET	I	DSP general-purpose port output interruption
23	AVDD	-	Power supply terminal
24	AVREF0	-	Ground connection
25-32		-	Ground connection
33	AVSS	-	Ground connection
34,35		-	Terminal (unused)
36		-	Power supply terminal
37,38	RX,TX	-	Terminal (unused)
39		-	Terminal (unused)
40	DSPCOM	I	Communication port with IC401
41	DSPSTS	O	Status communication port to IC401
42	DSPCLK	I	Clock input from IC401
43	DSPRDY	I	Ready signal input from IC401
44		-	Terminal (unused)
45,46	MIDIO_IN/OUT	I/O	DSP-microcomputer I/F
47	MICK	O	Clock signal to IC631
48	MICS	O	Chip select to IC631
49	MILP	O	DSP-microcomputer I/F
50	MIACK	O	DSP-microcomputer I/F
51,52		-	Terminal (unused)
53	DSPRST	O	DSP reset signal output
54-63		-	Terminal (unused)
64,65	CDTI/CDTO	I/O	CODEC-Microcomputer I/F
66	CCLK	O	Clock signal to IC601
67	CS	O	Chip select to IC601
68	XTS	O	OSC select
69,70		-	Terminal (unused)
71	PD	O	Reset signal input
72	GND	-	Ground connection
73-80		-	Terminal (unused)
81	VDD	-	Power supply terminal
82	3D-ON	-	Terminal (unused)
83	3D-ON	O	Switching terminal to where the surround channel is output
84	ANA/T-TONE	O	Test tone control
85	REF-MIX	O	Controlling terminal to where the LFE channel is output
86		-	Terminal (unused)
87	D.MUTE	O	MUTE for the digital OUT terminal
88	S.MUTE	O	MUTE for the audio signal
89		-	Terminal (unused)
90-93	ASW1-4	O	Digital input selection
94	TEST	-	Test terminal
95-100		-	Terminal (unused)

■ ZIVA3-PA1(IC501):AV DECODER

1.Terminal Layout



2.Block Diagrams



3.Pin Function (1/3)

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	TEST PIN0	-	Test pin	26	ARAM-DATA5	I/O	Non used
2	HDATA0	I/O	System control data I/O (IC301)	27	E-VDD	-	Power supply
3	HDATA1	I/O	System control data I/O (IC301)	28	ARAM-DATA6	I/O	Non used
4	HDATA2	I/O	System control data I/O (IC301)	29	E-VSS	-	Connect to GND
5	E-VDD	-	Power supply	30	ARAM-DATA7	I/O	Non used
6	HDATA3	I/O	System control data I/O (IC301)	31	ARAM-ADDR0	-	Connect to TP550
7	E-VSS	-	Connect to GND	32	ARAM-ADDR1	-	Connect to TP551
8	HDATA4	I/O	System control data I/O (IC301)	33	ARAM-ADDR2	-	Connect to TP552
9	HDATA5	I/O	System control data I/O (IC301)	34	ARAM-ADDR3	-	Connect to TP553
10	HDATA6	I/O	System control data I/O (IC301)	35	ARAM-ADDR4	-	Connect to TP554
11	HDATA7	I/O	System control data I/O (IC301)	36	E-VDD	-	Power supply
12	I-VDD	-	Power supply	37	ARAM-ADDR5	-	Connect to TP555
13	RST	I	Reset signal input	38	E-VSS	-	Connect to GND
14	I-VSS	-	Connect to GND	39	ARAM-ADDR6	-	Connect to TP556
15	WAIT	I	Wait control for IC509	40	I-VDD	-	Power supply
16	INT	O	Host interrupt output for ATAPI	41	ARAM-ADDR7	-	Connect to TP557
17	E-VDD	-	Power supply	42	I-VSS	-	Connect to GND
18	ARAM-OE	-	Connect to TP540	43	ARAM-ADDR8	-	Connect to TP558
19	E-VSS	-	Connect to GND	44	ARAM-ADDR9	-	Connect to TP559
20	ARAM-WE	-	Connect to TP541	45	ARAM-ADDR10	-	Connect to TP560
21	ARAM-DATA0	I/O	Non used	46	ARAM-ADDR11	-	Connect to TP561
22	ARAM-DATA1	I/O	Non used	47	E-VDD	-	Power supply
23	ARAM-DATA2	I/O	Non used	48	ARAM-ADDR12	-	Connect to TP562
24	ARAM-DATA3	I/O	Non used	49	E-VSS	-	Connect to GND
25	ARAM-DATA4	I/O	Non used	50	ARAM-ADDR13	-	Connect to TP563

Pin Function (2/3)

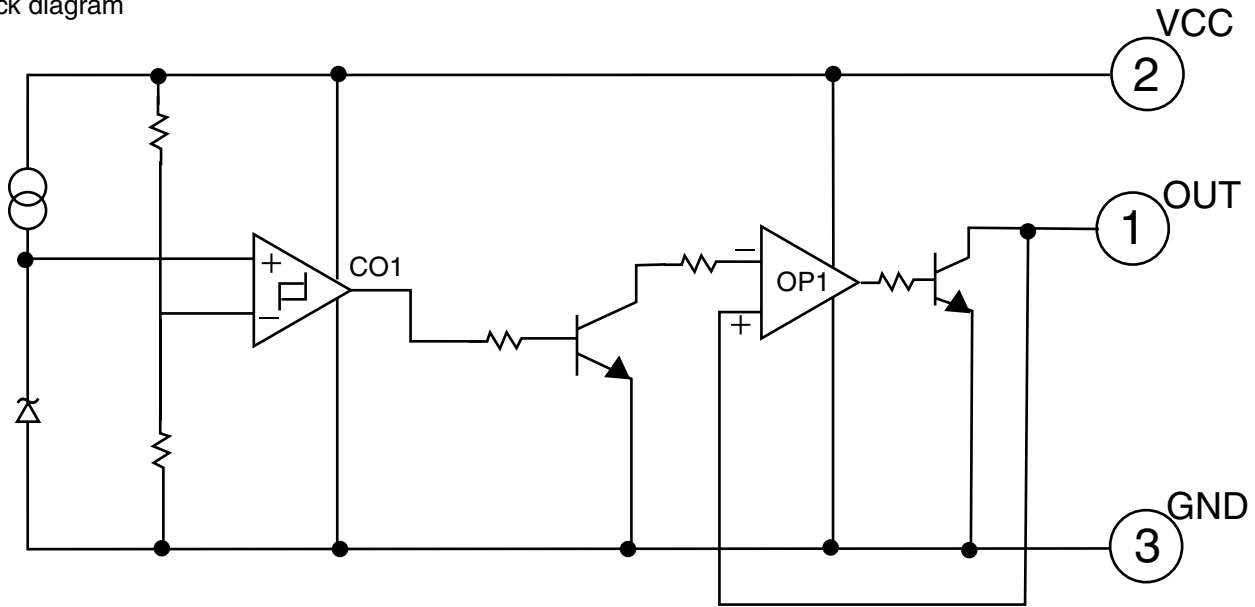
Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
51	ARAM-ADDR14	-	Connect to TP564	97	E-VSS	-	Connect to GND
52	TEST-PIN1	-	Test pin	98	M-ADDR11	O	Address output to IC508,504
53	M-DATA15	I/O	Data bus I/O to IC508,IC504	99	M-ADDR8	O	Address output to IC508,504
54	M-DATA0	I/O	Data bus I/O to IC508,IC504	100	M-ADDR10	O	Address output to IC508,504
55	E-VDD	-	Power supply	101	E-VDD	-	Power supply
56	M-DATA14	I/O	Data bus I/O to IC508,IC504	102	M-ADDR7	O	Address output to IC508,504
57	E-VSS	-	Connect to GND	103	E-VSS	-	Connect to GND
58	M-DATA1	I/O	Data bus I/O to IC508,IC504	104	M-ADDR0	O	Address output to IC508,504
59	M-DATA13	I/O	Data bus I/O to IC508,IC504	105	M-ADDR6	O	Address output to IC508,504
60	M-DATA2	I/O	Data bus I/O to IC508,IC504	106	M-ADDR1	O	Address output to IC508,504
61	E-VDD	-	Power supply	107	E-VDD	-	Power supply
62	M-DATA12	I/O	Data bus I/O to IC508,IC504	108	M-ADDR5	O	Address output to IC508,504
63	E-VSS	-	Connect to GND	109	E-VSS	-	Connect to GND
64	M-DATA3	I/O	Data bus I/O to IC508,IC504	110	M-ADDR2	O	Address output to IC508,504
65	I-VDD	-	Power supply	111	M-ADDR4	O	Address output to IC508,504
66	M-DATA11	I/O	Data bus I/O to IC508,IC504	112	M-ADDR3	O	Address output to IC508,504
67	I-VSS	-	Connect to GND	113	E-VDD	-	Power supply
68	M-DATA14	I/O	Data bus I/O to IC508,IC504	114	M-ADDR12	-	Connect to TP513
69	E-VDD	-	Power supply	115	E-VSS	-	Connect to GND
70	M-DATA10	I/O	Data bus I/O to IC508,IC504	116	M-ADDR13	-	Connect to TP514
71	E-VSS	-	Connect to GND	117	I-VDD	-	Power supply
72	M-DATA5	I/O	Data bus I/O to IC508,IC504	118	M-ADDR14	-	Connect to TP515
73	M-DATA9	I/O	Data bus I/O to IC508,IC504	119	I-VSS	-	Connect to GND
74	M-DATA6	I/O	Data bus I/O to IC508,IC504	120	M-ADDR15	-	Connect to TP516
75	E-VDD	-	Power supply	121	M-ADDR16	-	Connect to TP517
76	M-DATA8	I/O	Data bus I/O to IC508,IC504	122	M-ADDR17	-	Connect to TP518
77	E-VSS	-	Connect to GND	123	E-VDD	-	Power supply
78	M-DATA7	I/O	Data bus I/O to IC508,IC504	124	M-ADDR18	-	Connect to TP519
79	LDQM	O	Lower DQ mask enable	125	E-VSS	-	Connect to GND
80	UDQM	O	Upper DQ mask enable	126	M-ADDR19	-	Connect to TP520
81	E-VDD	-	Power supply	127	M-ADDR20	-	Connect to TP521
82	$\overline{\text{MWE}}$	O	Write enable	128	$\overline{\text{ROM-CS}}$	-	Connect to TP522
83	E-VSS	-	Connect to GND	129	TEST-PIN2	-	Test pin
84	SD-CLK	O	System clock signal output	130	OSD-CLK	-	Connect to TP523
85	$\overline{\text{SD-CAS}}$	O	column address strobe	131	OSD-DATA0	-	Connect to TP525
86	$\overline{\text{SD-RAS}}$	O	Row address strobe	132	OSD-DATA1	-	Connect to TP526
87	E-VDD	-	Power supply	133	TEST-PIN3	-	Test pin
88	$\overline{\text{SD-CS1}}$	O	Chip select output to IC508	134	E-VDD	-	Power supply
89	E-VSS	-	Connect to GND	135	OSD-DATA2	-	Connect to TP528
90	$\overline{\text{SD-CS0}}$	O	Chip select output to IC504	136	E-VSS	-	Connect to GND
91	I-VDD	-	Power supply	137	OSD-DATA3	-	Connect to TP529
92	$\overline{\text{EDO-CAS}}$	-	Connect to TP511	138	TEST-PIN4	-	Test pin
93	I-VSS	-	Connect to GND	139	OSD-BLK1	-	Connect to TP531
94	$\overline{\text{EDO-RAS}}$	-	Connect to TP512	140	OSDVC1	-	Connect to TP532
95	E-VDD	-	Power supply	141	TEST-PIN5	-	Test pin
96	M-ADDR9	O	Address output to IC508,504	142	VDATA0	O	DVD image signal output

Pin Function (3/3)

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
143	VDATA1	O	DVD image signal output	176	A-VDD	-	Connect to TP507
144	I-VDD	-	Power supply	177	VCLK	I/O	Dot clock signal output (27MHz)
145	VDATA2	O	DVD image signal output	178	SYCLK	-	Connect to TP505
146	I-VSS	-	Connect to GND	179	A-VSS	-	Connect to GND
147	TEST-PIN6	-	Test pin	180	DVD-DATA0	I	ATAPI data I/O to IC301
148	VDATA3	O	DVD image signal output	181	E-VDD	-	Power supply
149	E-VDD	-	Power supply	182	DVD-DATA1	I	ATAPI data I/O to IC301
150	VDATA4	O	DVD image signal output	183	E-VSS	-	Connect to GND
151	E-VSS	-	Connect to GND	184	DVD-DATA2	I	ATAPI data I/O to IC301
152	VDATA5	O	DVD image signal output	185	DVD-DATA3	I	ATAPI data I/O to IC301
153	TEST-PIN7	-	Test pin	186	DVD-DATA4	I	ATAPI data I/O to IC301
154	VDATA6	O	DVD image signal output	187	DVD-DATA5	I	ATAPI data I/O to IC301
155	VDATA7	O	DVD image signal output	188	DVD-DATA6	I	ATAPI data I/O to IC301
156	TEST-PIN8	-	Test pin	189	DVD-DATA7	I/O	ATAPI data I/O to IC301
157	HSYNC	I/O	Horizontal synchronous signal output	190	TEST-PIN10	-	Test pin
158	VSYNC	I/O	Vertical synchronous signal output	191	V-REQUEST	O	Master/Sleeve Selection for ATAPI
159	IEC-958	O	Digital audio data output	192	V-STROBE	I	Host address for ATAPI
160	E-VDD	-	Power supply	193	I-VDD	-	Power supply
161	DA-DATA0	O	Data output to IC702	194	A-REQUEST	-	Connect to TP539
162	E-VSS	-	Connect to GND	195	I-VSS	-	Connect to GND
163	DA-DATA1	O	Data output to IC702	196	V-DACK	I	Host interrupt input for ATAPI
164	DA-DATA2	O	Data output to IC702	197	E-VDD	-	Power supply
165	DA-DATA3	O	Data output to IC702	198	SECT-SYNC	I	Host write for ATAPI
166	DA-LRCK	O	L/R clock output to IC702	199	E-VSS	-	Connect to GND
167	DA-BCK	O	Bit clock output to IC702	200	ERROR	-	Connect to GND
168	I-VDD	-	Power supply	201	HOST-SEL	-	Connect to GND
169	DA-XCK	-	Non connect	202	HADDR0	I	System control address input
170	I-VSS	-	Connect to GND	203	HADDR1	I	System control address input
171	DAI-DATA	-	Connect to TP501	204	HADDR2	I	System control address input
172	DAI-LRCK	I	L/R clock input from IC702	205	DTACK-SEL	-	Connect to GND
173	DAI-BCK	I	Bit clock input from IC702	206	$\overline{\text{CS}}$	I	Chip select for ZIVA
174	TEST-PIN9	-	Test pin	207	$\overline{\text{R/W}}$	I	Write enable
175	CLK-SEL	-	Connect to GND	208	$\overline{\text{RD}}$	I	Read enable

■ IC-PST9140-T (IC717) : RESET IC

1. block diagram

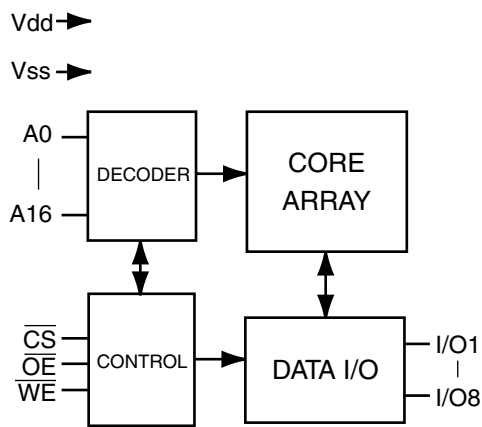


■ W24L011AJ-15(IC641): SDRAM

1. Terminal layout

A0	1	32	A16
A1	2	31	A15
A2	3	30	A14
A3	4	29	A13
CS	5	28	OE
I/O1	6	27	I/O8
I/O2	7	26	I/O7
VDD	8	25	VSS
VSS	9	24	VDD
I/O3	10	23	I/O6
I/O4	11	22	I/O5
WE	12	21	A12
A4	13	20	A11
A5	14	19	A10
A6	15	18	A9
A7	16	17	A8

2. Block diagram

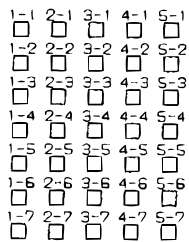
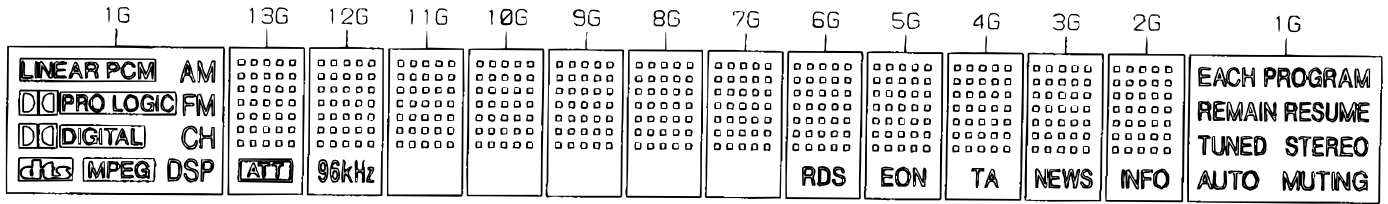


3. Pin function

Symbol	Description
A0-A16	Address input
I/O1-I/O8	Data input/output
CS	Chip select input
WE	Write enable input
OE	Output enable input
Vdd	Power supply terminal
Vss	Ground connection

Internal connection of FL display tube

■ QLF0049-001(DI831):FL DISPLAY TUBE



(13G~26G)

PIN CONNECTION

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
CONNECTION	F	F	N	N	N	N	N	N	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P

PIN NO.	5	5	5	5	5	5	5	5	6	6	6	
CONNECTION	8	7	5	5	4	3	2	1	N	N	F	F

- NOTE
- 1) F1, F2 --- Filament
 - 2) NP ----- No pin
 - 3) NC ----- No connection
 - 4) DL ----- Datum Line
 - 5) 1G~13G --- Grid

ANODE CONNECTION

	13G	12G	11G	10G	9G	8G	7G	6G	5G	4G	3G	2G	1G
P1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	EACH
P2	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	PROGRAM
P3	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	REMAIN
P4	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	RESUME
P5	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	TUNED
P6	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	STEREO
P7	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	AUTO
P8	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	MUTING
P9	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	LINEAR PCM
P10	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	AM
P11	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	DIGI PRO LOGIC
P12	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	FM
P13	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	DIGITAL
P14	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	CH
P15	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	dts
P16	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	MPEG
P17	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	DSP
P18	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	-
P19	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	-
P20	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	-
P21	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	-
P22	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	-
P23	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	-
P24	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	-
P25	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	-
P26	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	-
P27	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	-
P28	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	-
P29	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	-
P30	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	-
P31	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	-
P32	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	-
P33	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	-
P34	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	-
P35	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	-
P36	ATT	96kHz	-	-	-	-	-	-	RDS EON	TA	NEWS	INFO	-

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